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# 7—4 New A/D conversion technique for smart image sensor

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## Abstract

In this paper, we propose a new method of 8bit Analog to Digital Conversion on an image sensor. In this method, we use small 1bit comparator which detects each bit during integration, repeatedly. Consequently, both the A/D conversion and the integration of the pixel value can be done in parallel.

We have designed a prototype by using column parallel architecture. The prototype outputs analog value and 8 bit digital value of pixel data. It has 32 × 16 pixels and digital memory for each pixel. We describe the processing scheme of our ADC and the circuit and layout design of the prototype. We show results of some experiments.

## 1 Introduction

Integration of sensing and processing is a novel approach to enhance the performance of image sensor and to extract primitive information such as motion and edge [1] [4]. The integration makes use of parallel nature of image signal on the focal plane so that the processing gets remarkably faster compared to ordinary image processing systems which are based on a traditional sense-read-and-process paradigm.

In this paper, we propose a new method of 8bit Analog to Digital Converter (ADC) on an image sensor by using non-destructive read out during integration. 8bit ADC can be done by using small 1bit comparator which detects each bit, repeatedly.

We have designed a prototype by using column parallel architecture. The prototype has 32 × 16 pixels and 8bit memory for each pixel. We describe the processing scheme of our ADC and the circuit and layout design of the prototype.

## 2 A/D conversion algorithm

Figure 1 shows the comparison between the conventional method and the proposed method. In the conventional method, ADC is done after the integration of PD charge. On the other hand, the processing of our proposal is divided into 4 steps (s1.s2.s3.s4) during the integration of PD value. 2 bit of pixel value is determined at each step. Therefore 8 bit value is determined when the integration is finished. Because we use 1 bit comparator for 8bit A/D conversion repeatedly, the processing circuit of A/D conversion is very small.

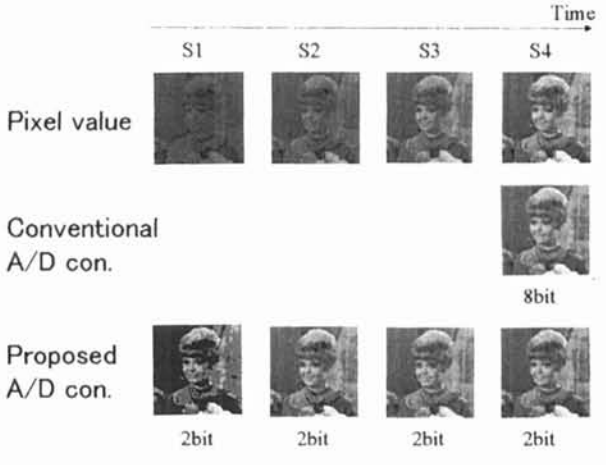


Figure 1: Comparison between the conventional ADC and the proposed ADC

In our proposal, the interval of each step is not equal. The processing of s1, s2, s3, s4 is done when the integration time is 1/8, 1/4, 1/2 ,1 frame, respectively. By this scheme, the number of the reference values are reduced from 14 to 8 so that the peripheral circuit to make the threshold voltage is also small. Table 1 shows the reference values for each sub-frame.

Figure 2 shows an example of the proposed method when the final pixel value is 200. Because the object is not moving, pixel values for s1, s2, s3 and s4 are 25, 50, 100 and 200, respectively. Table 2 shows the threshold of each step and the result of A/D conversion.

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Table 2: Threshold of each bit and the result of ADC

| result | | MSB bit8 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | LSB bit1 | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | |
| s1(1/8) | th1 | 16 | | | | | | | | =16 |
| | th2 | 16 | +8 | | | | | | | =24 |
| s2(1/4) | th3 | 32 | +16 | +8 | | | | | | =56 |
| | th4 | 32 | +16 | 0 | +4 | | | | | =52 |
| s3(1/2) | th5 | 64 | +32 | 0 | 0 | +4 | | | | =100 |
| | th6 | 64 | +32 | 0 | 0 | +4 | +2 | | | =102 |
| s4( 1 ) | th7 | 128 | +64 | 0 | 0 | +8 | 0 | +2 | | =202 |
| | th8 | 128 | +64 | 0 | 0 | +8 | 0 | 0 | +1 | =201 |

Table 1: Reference potential for each sub-frame (s1. s2. s3. s4)

| | MSB bit8 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | LSB bit1 |
|---|---|---|---|---|---|---|---|---|
| s1(1/8) | 16 | 8 | | | | | | |
| s2(1/4) | 32 | 16 | 8 | 4 | | | | |
| s3(1/2) | 64 | 32 | 16 | 8 | 4 | 2 | | |
| s4( 1 ) | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |

## 3 Computer simulation of the proposed ADC

Figure 3 shows the simulation results of our A/D conversion when the speed of the object is 12 pixels / frame and 120 pixels / frame. Fig.(a) and (c) are the results of the conventional method (A/D conversion after integration) and Fig.(b) and (c) are the results of the proposed method (A/D conversion during integration). It appeared that the results of the proposed method is much clear compared to the conventional approach.

In our proposal. higher bit (ex. MSB) is determined when the integration time is shorter. Therefore the motion blur is reduced as shown in Fig.3.

## 4 Circuit design of on-sensor A/D conversion

We have designed a prototype chip based on column parallel architecture. Figure 4 shows the block diagram of the on-sensor A/D conversion. The prototype is divided into three part which are transducer array. 8bit digital memory array and A/D conversion circuits. The pixels on each column shares one A/D conversion circuit. Using two vertical shift

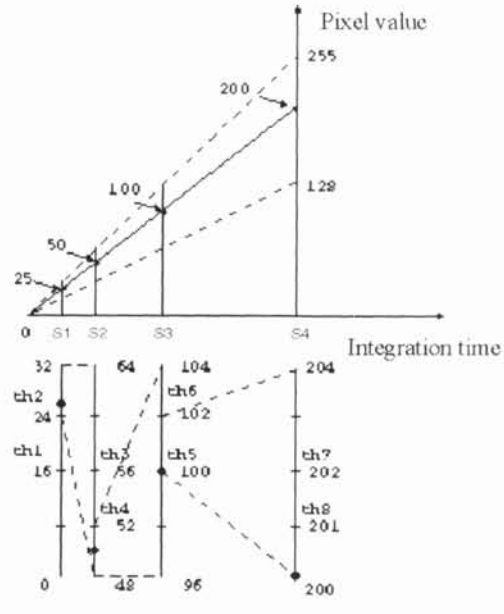


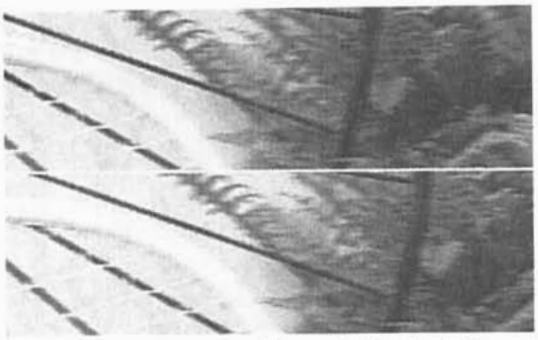

Figure 2: Example of our ADC method when the pixel value is 200

registers. the pixels and the memories are scanned line by line. Power circuit between two vertical shift registers supplies the reference voltage for D/A converter in the processing circuit.

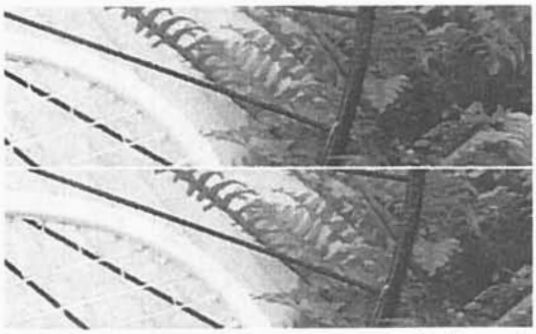
Figure 5 shows the circuits of the prototype. Each pixel has only a transducer and a separate corresponding 8bit digital memory and a processing circuit shared by the pixels on the column. The processing circuit has sample & hold circuit. comparator. temporal 2 bit memory. D/A converter and switch circuit.

## 5 Prototype chip and experiment

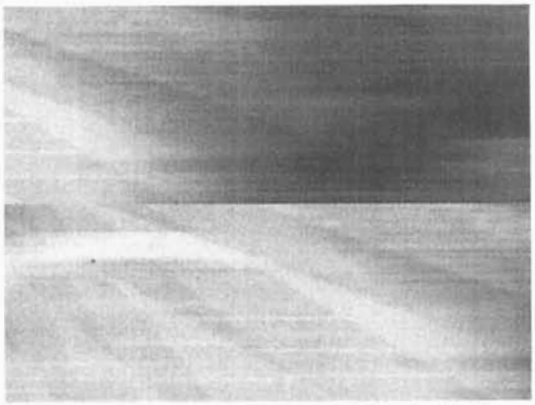
We has fabricated a prototype chip by using 2-poly 3-metal 0.6 $\mu m$ CMOS process. Table 3 shows



(a)conventional method (speed 12 pixels/frame)



(b)proposed method (speed 12 pixels/frame)



(c)conventional method (speed 120 pixels/frame)

(d)proposed method (speed 120 pixels/frame)

Figure 3: Simulation result of A/D conversion: conventional method: pixel intensity is determined after integration. proposed method: pixel intensity is determined during integration.

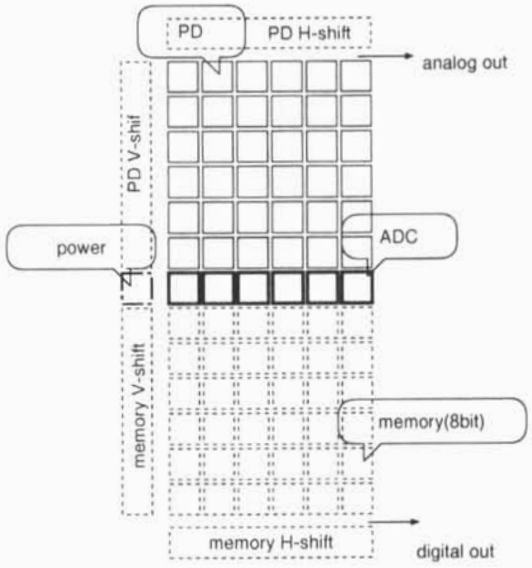



Figure 4: Block diagram of the prototype chip

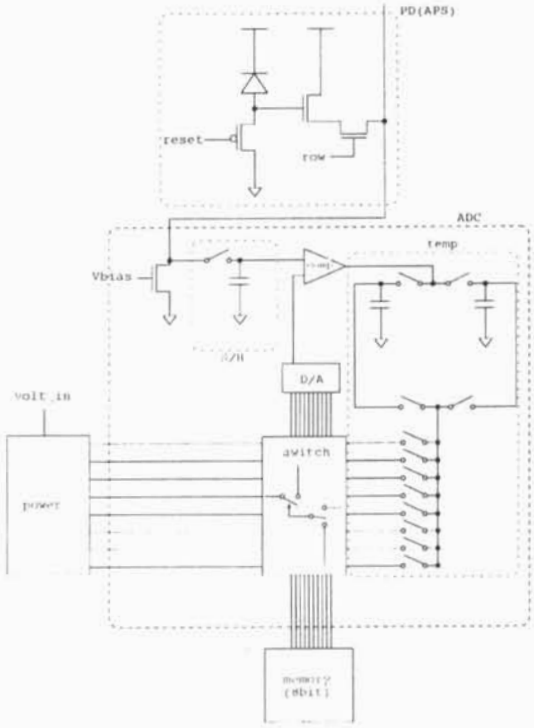



Figure 5: Circuit for a pixel

Table 3: Outline of the prototype of column parallel architecture

| | |
|---|---|
| number of pixels | 32 × 16 |
| process($\mu m$) | 0.6 |
| chip size($mm^2$) | 4.5 × 4.5 |
| transducer($\mu m^2$/pixel) | 20× 20 |
| memory($\mu m^2$/pixel) | 63 × 73 |
| processing($\mu m^2$/column) | 63 × 615 |
| transducer(Tr./pixel) | 3 |
| memory(Tr./pixel) | 72 |
| processing(Tr./column) | 266 |
| fill factor(%) | 41.2 |
| power (V) | 5 |

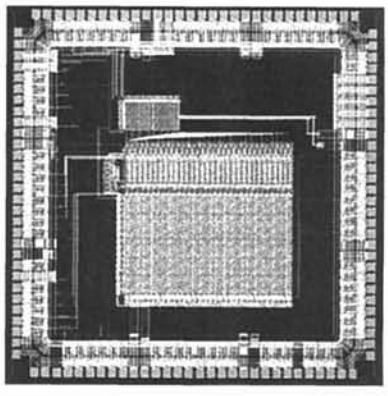


Figure 6: Layout of the prototype

the outline of the prototype. The sensor has 32 x 16 pixels and fill factor is 41.2%. Figure 6 shows a layout of the prototype and Figure 7 shows an photograph of the prototype.

Figure 8 shows the analog output images obtained by the prototype when "sensor" is moving from right to left.

## 6 Conclusion

In this paper, we propose a new method of on-sensor A/D conversion for digital smart image sensor. In the method, integration of pixel value and A/D conversion can be done in parallel. We have designed and implemented a new prototype chip which has 32 × 16 pixes. The prototype is now under further experiments.

The VLSI chip has been fabricated in the chip fabrication program of VLSI Design and Education Center(VDEC), the University of Tokyo with the collaboration by Rohm Corporation and Toppan Printing Corporation.

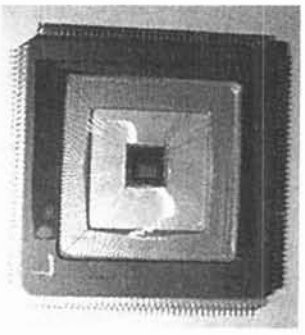


Figure 7: Prototype chip

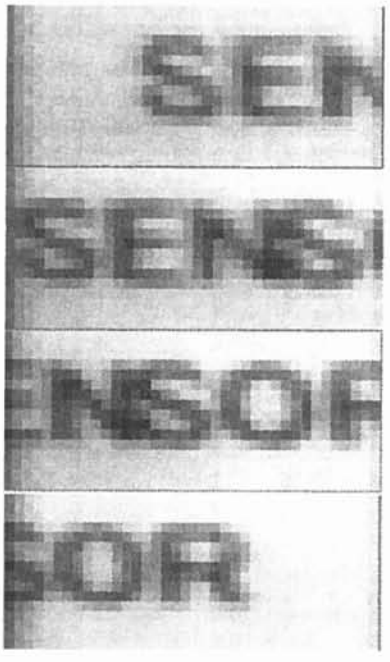


Figure 8: Analog output images (character "sensor")

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