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11—1 A New Image Sensor With Space Variant Sampling Control On A Focal Plane

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Abstract

We propose a new sampling control system on image sensor. Contrary to the random access pixels, the proposed sensor is able to read out spatially variant pixels at high speed, without inputting pixel address for each access. The sampling positions can be changed dynamically by rewriting the sampling position memory. Since the proposed sensor has sampling position memory that stores the sampling control order, it is able to easily control sampling position. We can achieve any spatially varying sampling patterns.

1 Introduction

In biological vision, the retina is equivalent to the imaging sensor. It is organized into a space-variant sampling structure including a high-resolution, small central fovea and a periphery the resolution of which linearly decreases in steps. By this characteristic, it is able to centralize and distribute the processing loads in the earliest stage of vision.

Therefore it is essential for smart sensing to integrate functions of spatially variant flexible sampling control onto a computational sensor. The integration on the sensor focal plane results in enhancement of performance of an image sensor.

In this paper, we propose a new sampling control system on image sensor for space-variant sensing. We will present the principles, circuit designs, a prototype of the sensor and active control system using sampling control sensor.

2 Spatially Variant Sampling

Spatially variant sampling is a strategy for image acquisition that has been demonstrated to be very interesting for image processing. Traditional machine vision applications have often been hampered by the need of processing huge amounts of data, because they cannot extract only the information required to accomplish specific tasks. It is essential for the vision systems to have specific mechanisms for data reduction and selection that plays major role to simplify visual computation.

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Spatially variant sampling enable the vision system to select among visual data the relevant information and ignore irrelevant details to the vision systems. This strategy leads to a data reduction that has a direct impact on the system performance, especially speed, and on the complexity of the computer architecture to process the image and it is crucial when a real time performance is required.

3 Flexible Sampling Control On Sensor

In this paper a new space variant sampling control which uses sampling position memory is proposed. Each element of the sampling position memory corresponds to each pixel and it contains a binary data to determine the pixel is read out. Thus there is no need to input pixel address for each access, and pixel value can be read out at high speed. Fig.2 illustrates a diagram of the sensor.

A smart scanning shift register (Fig.1) [1] is used to selectively read out pixel values, and the binary data of the memory is used as a control signal. Examples of the read out mode are illustrated in Fig.3 and Fig.4. Sub-sampling or block access(Fig.3) are easily available. By the smart scanning, only those pixels, the memory elements of which are H, are read out in a compact sequence. the pixels, the memory of which are L, are immediately skipped. Sampling at high resolution at center and low resolution at peripheral pixels, similar to foveated vision(Fig.4), are also available. Fig.4 is the images obtained by the simulation. The left is the original image and the right is the simulated image consists of center portion at normal resolution(128pixel radius) and peripheral radially sub-sampled.

By rewriting the sampling position memory, the position of the fovea can be freely moved on the sensor. Therefore if we use the sensor in active vision systems, the fast feature extraction is possible.

4 Circuit Design of A Prototype

Fig.6 shows the block diagram of the sampling control sensor. This sensor mainly consists of two parts. They are pixel array and sampling position

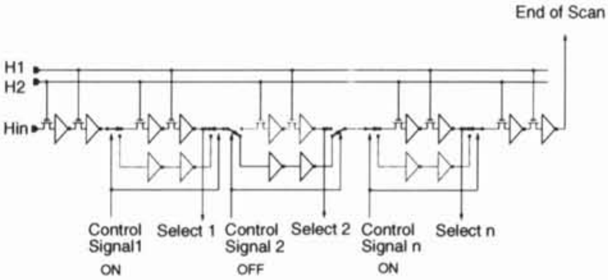

Figure 1: Smart scanning shift register.

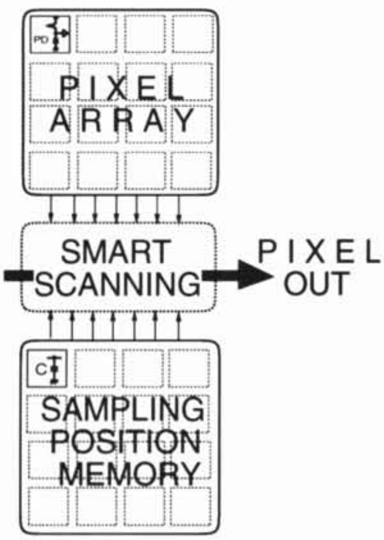

Figure 2: Diagram of sampling control system.

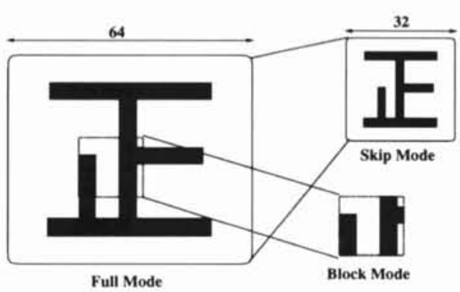

Figure 3: Block and skip access mode.

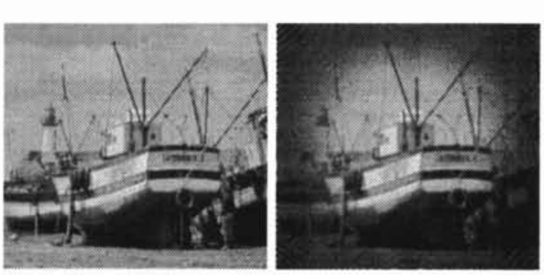

Figure 4: Fovea-like output image.

memory. Fig.5 shows an analog circuit of the pixel and the memory.

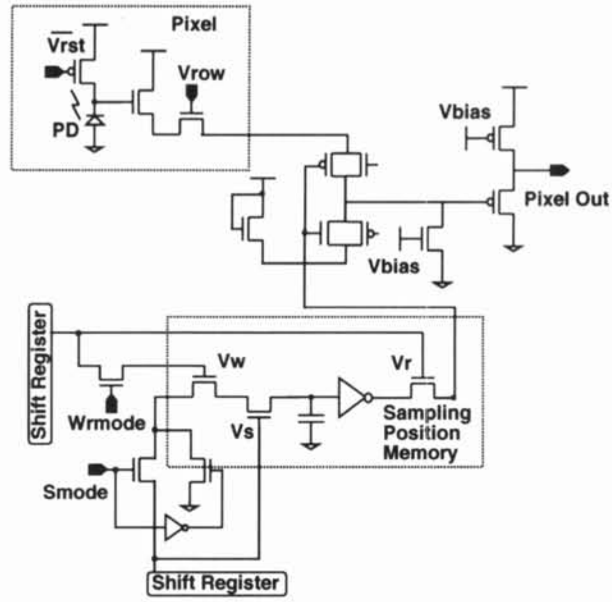

Figure 5: A design of pixel circuit and sampling position memory.

Pixel array consists of pixel circuits. A pixel circuit contains three transistors, so that we can get a practical fill factor. Pixel values are transmitted to the horizontal shift register, and selected based on memory values of sampling position memory. And values of only the selected pixels are read out.

The proposed sensor has two different type of horizontal shift registers: a normal and a smart scanning shift registers. One of the two is selected by the mode selection signal. In the case of the smart scanning shift register, only the selected pixels are read out and non-selected pixels are skipped without reading. In order to reconstruct the output image, address data is required, wherein known sampling position may be used.

Sampling position memory mainly consists of a capacitance and switches and can be dynamically rewritten.

Both pixel array and sampling position memory have vertical shift registers which are driven by the same signals to select corresponding pair of rows. The sensor has another horizontal shift register at the bottom so that it can rewrite independently sampling position memory within a horizontal scanning period. The bottom horizontal shift register can also read out the control bits as flag signals.

In order to write control bits in sampling position memory, the output signal from the horizontal shift register is controlled by sample selection signal (*Smode*). If *Smode* is "1", the output signal from the bottom shift register is transmitted to the memory and its value is set to "1". If *Smode* is "0", the memory is reset. Using *wrmode* signal, the signal from shift register is input only at the time of writing.

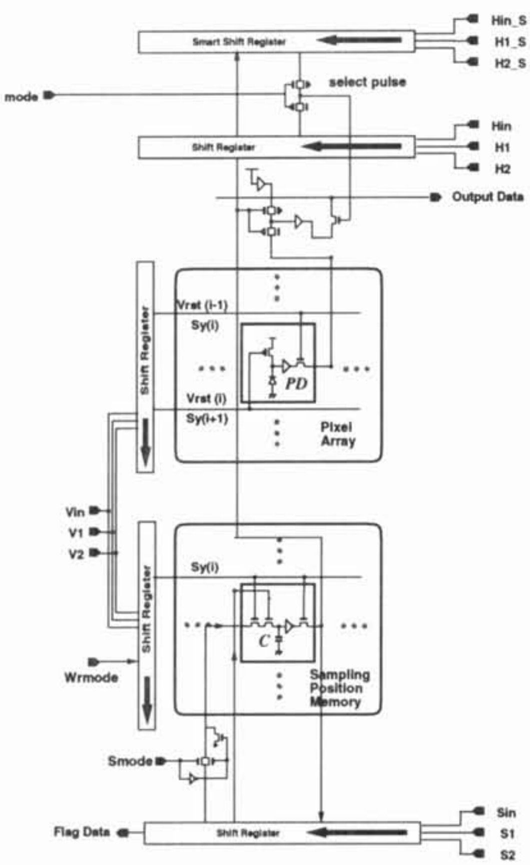

Figure 6: Block diagram of sampling control image sensor.

5 A Prototype Chip

Fig.7 shows a chip layout of a prototype, and Fig.8 shows a picture of the prototype chip. Table 1 shows the characteristics of it. It is designed under 1-poly 2-metal CMOS 0.7μm rule. Table 1 shows the characteristics of the prototype. The number of the transistors in the pixel array element is three, which is equal to the conventional CMOS sensor [2]. Number of pixels is 64×64.

Fig.9 shows an output image obtained by the prototype. Fig.10 shows images obtained by the prototype in skip or block access mode. The left is the image when every other column is sampled and read out by the smart horizontal shift register. The right is the one when every other column and every other row is sampled. The center is the one when specific block areas are selectively sampled. The skipped pixels are shown black.

Fig.11 shows a example of the varieties of sample-controlled image. The left images are obtained by the prototype at smart scanning mode. The center images are the flag data in the sampling position memory. The right are reconstructed images. This example shows a retina like sampling where the density changes high to low from the center to the peripheral.

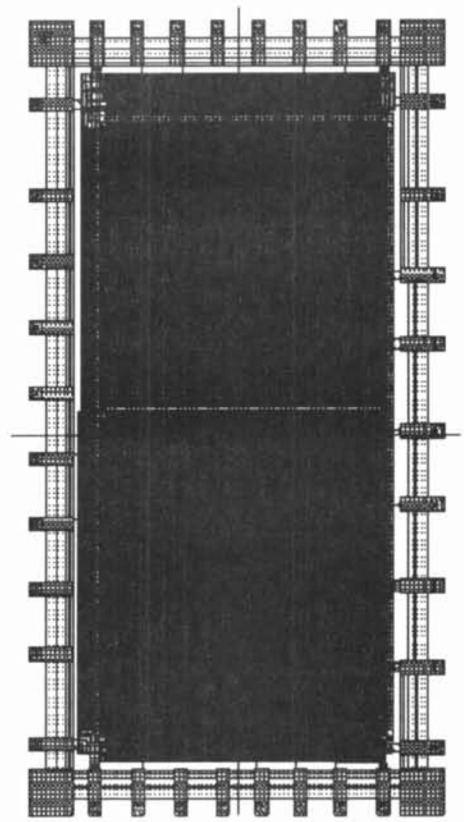

Figure 7: Chip layout of a prototype.

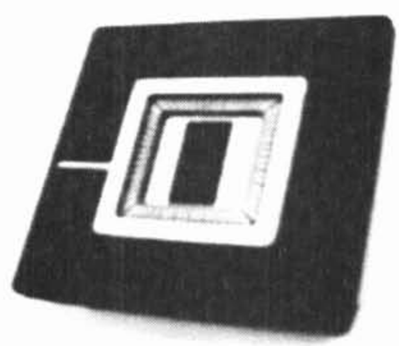

Figure 8: A prototype chip.

Figure 9: An image obtained by the prototype.

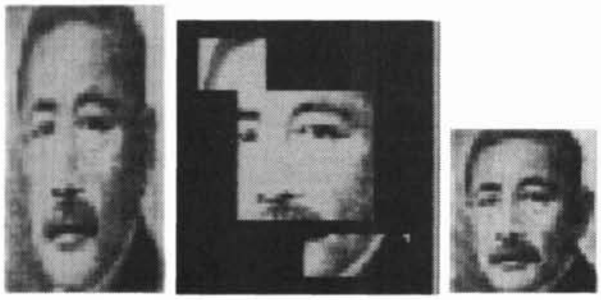

Figure 10: Output images selectively sampled by the prototype.

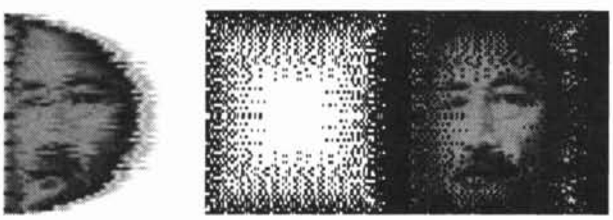

Figure 11: Reconstruction of a retina-like sampling image

6 Active sampling control system

Sampling control sensor is able to dynamically change patterns of output image by rewriting the sampling position memory. Therefore, it is able to track moving object with space variant resolution or time variant resolution.

- Space variant resolution

  By sampling at high resolution at center and low resolution at peripheral pixels, retina-like output images are available. By linking to object tracking program, the position of the fovea can be freely moved on the sensor(Fig.12).

- Time variant resolution

  Sampling sensor can get variant time-resolution images(Fig.12). In Fig.12, time-resolution is divided into 3 steps, selected pixels are outputted every frame at center, every 2 frames at middle, and every 3 frames at circumference. Therefore, it is needed to rewrite sampling position memory every frame. In this pattern, the position of the fovea also can be freely moved on the sensor by linking to object tracking program.

Table 1: Characteristics of the prototype.

♯ of pixels	64 × 64 pixels
♯ of transistors	pixel : 3 trs. / pixel
	memory : 9 trs. / pixel
fill factor	25%
power dissipation	5mW / chip

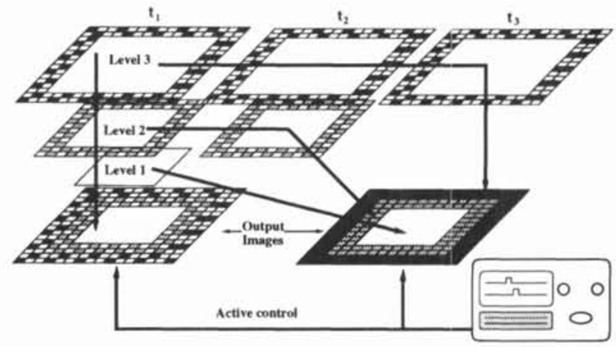

Figure 12: Active sampling position control

7 Conclusions

Proposed is a new image sensor with space-variant flexible sampling control integrated on a sensor focal plane. The principles of the processing, the designs of the circuits based on column parallel architecture, and the prototype chip have been presented.

The following advantages is obtained from the sensor.

- It can set arbitrary sampling positions.
- Sampling such as high resolution at center and low resolution at peripheral pixels, similar to foveated vision, is available.
- It can also output in blocks or by regular subsampling patterns.

The prototype is now under further experiments in a system using FPGA.

References

[1] K.Aizawa, Y.Egi, T.Hamamoto, M.Hatori,M.Abe H.Maruyama and H.Otake, "Computational Image Sensor For On Sensor Compression", *IEEE Trans.on Electron Devices Special Issue "Solid State Image Sensors"*, Vol.44, No.10, pp. 1724–1730, 1997.

[2] F.Ando, K.Taketoshi, K.Nakamura and M.Imai, "AMI; A New Amplifying Solid State Imager", *ITEJ*, Vol.41, No.11, pp. 1075–1082, 1987.