3—12

New design and implementation of on-sensor-compression

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Abstract

We have been investigating a novel integration of sensing and compression on an image sensor. By the integration, number of pixels in the image signal that has to be readout from the sensor can be significantly reduced, and the integration can consequently increase the pixel rate of the sensor.

In this paper, we present a new compression sensor which has 128×128 pixels. We have designed and implemented the new prototype by using a column parallel architecture. We show the some experimental results obtained by the prototype.

1 Introduction

Integration of processing and sensing is a novel approach to very fast image processing and also to augmenting performances of an image sensor. We have been investigating smart image sensors on which the image signal is compressed [1]–[3]. The integration significantly reduces pixel data read out from the sensor. Thus, the compression sensor can capture the images at the higher pixel rate which the traditional sensor can not handle.

In this paper, we present a new compression sensor which has 128x128 pixels. The new prototype is designed by a column parallel architecture which shares processing modules among pixels in the column. Main benefits of the architecture are high fill factor and low power dissipation. The circuit and layout designs are renewed to achieve much lower power dissipation and higher processing speed beyond the performance of the previous prototypes[1]-[3] of which the resolution is 32x32 pixels. An address encoder is newly implemented on this prototype.

2 Conditional replenishment

We employ conditional replenishment (CR) for the compression algorithm on the image sensor. CR detects and encodes only moving pixels to compress image signals.

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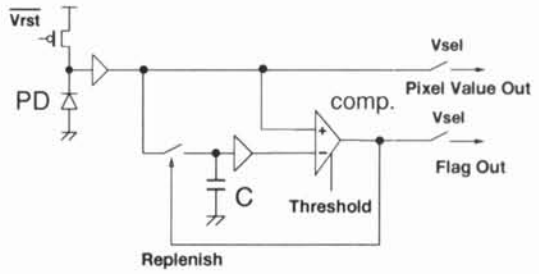

Figure 1: Description of coding algorithm in each pixel by conditional replenishment

Figure 1 illustrates the processing scheme of CR. Motion is detected in each pixel when the magnitude of the difference between the pixel intensity and the memorized value exceeds a threshold. If the motion is detected, the pixel intensity and its addresses are output and the value in the memory is replenished by the pixel intensity. Therefore, the memorized value equals to the intensity last output from the pixel. Although CR is rather simple, its compression performance gets higher when the frame rate is higher.

3 Design and implementation of new compression sensor

We have designed the new 128x128 pixels compression sensor by using the column parallel architecture. Figure 2 shows a block diagram of the new compression sensor. Pixel, memory and processing elements are separated on the chip and pixels of a column share a processing element. Because of this architecture, fill factor keeps the same level of an ordinary CMOS sensor and power dissipation is much improved compared to the pixel parallel architecture[1][2].

It has three vertical shift registers, two horizontal shift registers and address encoder except three core elements. The upper horizontal shift register has two scanning modes that are normal and smart scanning, and one of the two is selected by a mode signal. Figure 3 shows a circuit of the smart shift register. In the case of the normal scanning, upper paths are selected for all pixels, and all pixels are read out.

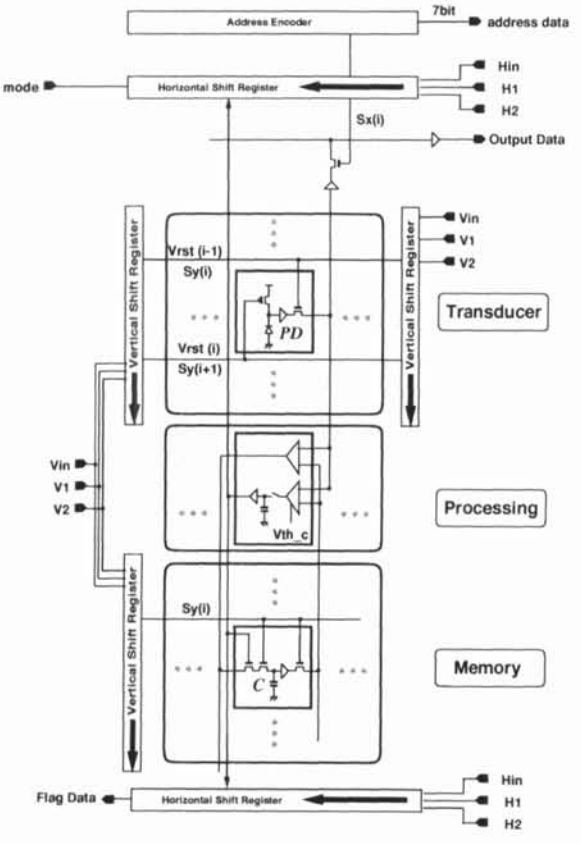

Figure 2: Block diagram of new compression sensor

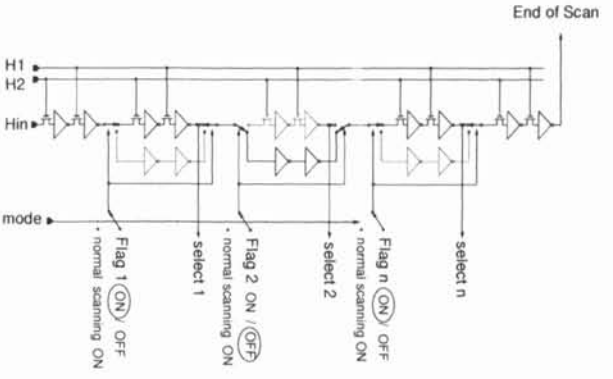

Figure 3: Smart horizontal shift register

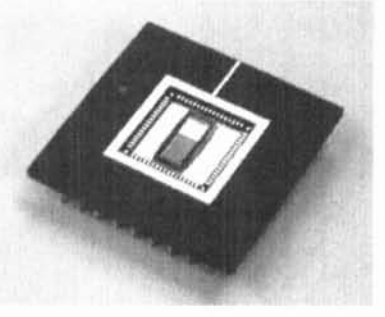

Figure 4: Prototype chip

In the case of the smart scanning, if the flag signal is off, the bottom path is selected to skip the pixel without reading. It outputs only the activated pixels without blank space in the output sequence.

When the smart scanning mode is selected, we use one of the two address information for reconstruction. One is flag signal output by the bottom high speed horizontal shift register shown in Fig.2. The other is 7bits addresses output by the address encoder.

We have fabricated the new compression sensor by using 1-poly 2-metal CMOS $0.7\mu m$ process. Table 1 shows the outline of both our first column parallel architecture[3] and the new one. Power dissipation and processing speed are much improved. Figure 4 shows a photograph of the packaged chip.

4 Experiments

4.1 Output signals of both normal and smart scanning modes

Figure 5 shows image outputs and flag signals obtained by the prototype. In the experiments, the texture projected onto the focal plane is moving horizontally at high speed.

Figure 5(a) shows the output signals of the normal scanning mode. The vertical edges of the texture activate the flags clearly. Figure 5(b) shows the output signals of the smart scanning mode. Because the smart shift register skips non-activated pixels, the intensities of the activated pixels are packed to the left side of the sequence.

4.2 Real-time reconstruction using flag signals

Figure 6 shows example frames of real-time reconstruction. We use the flag signals as the address information of the activated pixels. The frames are reconstructed by a SGI workstation in real time. In this experiment, the prototype operates at 60 frames / second and the pixel and flag signals are continually captured as NTSC component signals. All frames output by the prototype sensor is not used for the reconstruction due to a limited performance of the workstation. Therefore some corruptions of the reconstructed images are observed.

4.3 Experiments of a single pixel circuit

Figure 7 shows the response of a single pixel circuit when a LED driven by a sinusoidal wave is used as a light source. Figure 7 shows the results under three thresholds for motion detection. In this experiments, the reconstructed values are equal to

Table 1: Comparison between first[3] and new prototypes of the column parallel architecture

	first prototype[3]	new prototype
number of pixels[pixels]	32 × 32	128 ×128
CMOS process[μm]	1.0	0.7
die size[mm^2]	3.6 × 6.4	3.9×8.3
pixel size		
transducer[μm^2/pixel]	60 × 60	19.2×19.2
memory[μm^2/pixel]	60 × 65	19.2×30.0
processing[μm^2/pixel]	60 × 244	19.2 ×290.7
fill factor[%]	38.5	22.3
power dissipation[mW/column]	1.5	0.3
processing speed[μs / row]	≥ 2	≥ 0.5

the memory values. According to increase of the threshold control voltage (logical threshold voltage decreases), the memory values get closer to the pixel values. We have verified that the processing circuits can operate at more than 5000 frames /second.

5 Conclusion

In this paper, we describe a compression sensor based on the column parallel architecture. We have designed and implemented a new prototype which has 128x128 pixels. The some experimental results obtained by the prototype are shown.

The real-time reconstruction system using FPGA is now under investigation.

References

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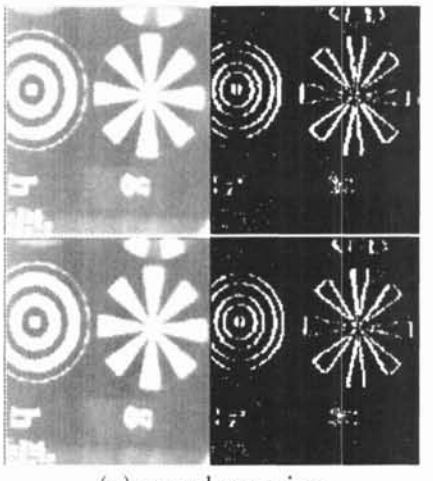
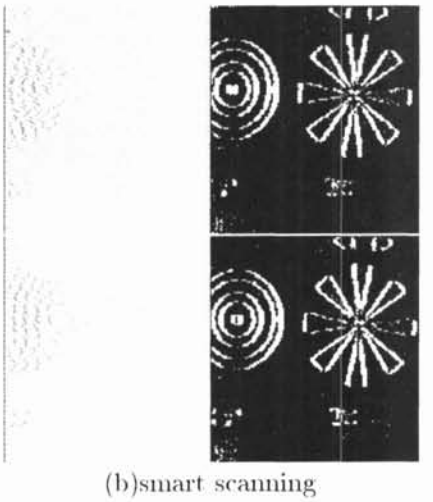


(a)normal scanning



(b)smart scanning

Figure 5: Images obtained by the prototype when the texture is moving horizontally at high speed.; The left figures show pixel intensity, and the right figures show flag signal.

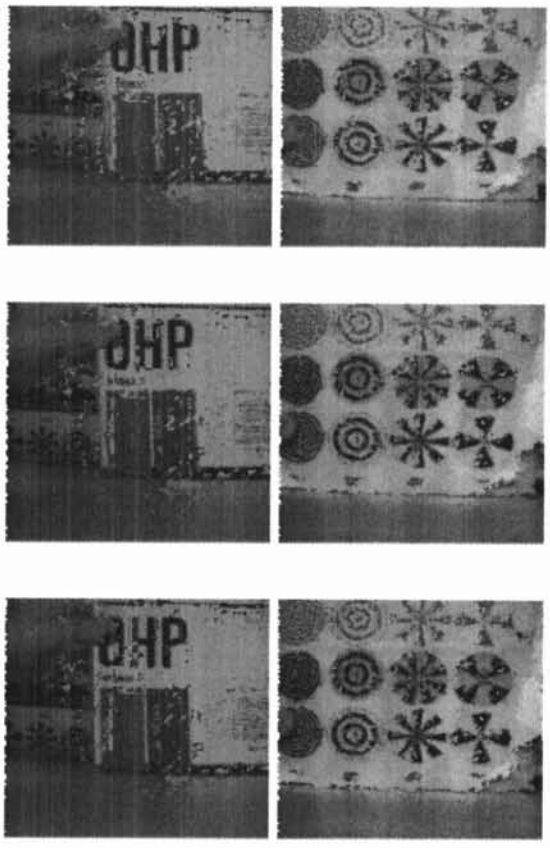
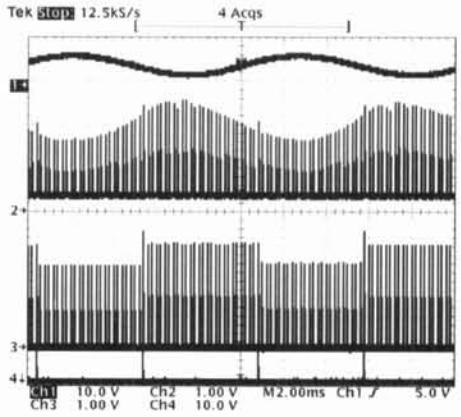
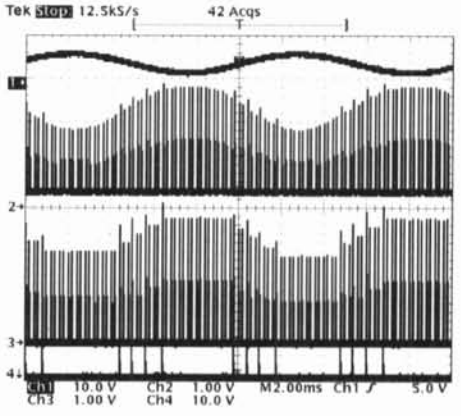


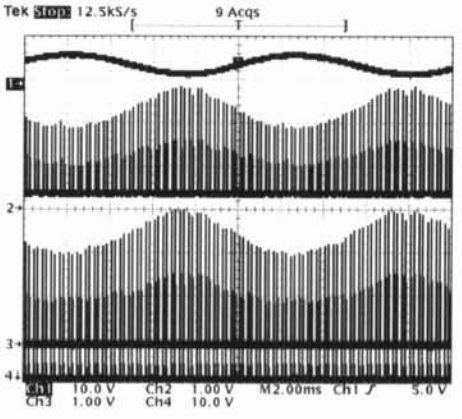
Figure 6: Example frames of real-time reconstruction by using a workstation



(a)Vth=1.0V



(b)Vth=2.0V



(c)Vth=3.5V

Figure 7: Response of a single pixel circuit under various thresholds for change detection when processing speed is equivalent to 5000 frames / second. : From top to bottom waves in (a)(b)(c); LED driving voltage, pixel value, memory value and flag signals, respectively.