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EXTRACTION OF TOPOLOGICAL FEATURES OF INTEGRATED CIRCUIT FROM GREY-SCALE IMAGE

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Abstract

A method for integrated circuit image processing is proposed. It makes easier a topology reconstruction process and is able to successfully process images scanned from an integrated circuit layer. Implementation of image analysis techniques accelerates the process of reverse engineering as well as a quality control and analysis of integrated circuits. The idea of sequential raster-to-vector and vector-to-raster transforms was implemented.

1 Introduction

Reverse engineering is widely used to check quality and to design advanced integrated circuits (IC)[1-3]. Its principal idea is to use already produced item during design of a new one. The process is performed in the following way: IC is scanned with producing a digital image, the image is analysed to recognise IC elements and their location, and finally all elements are combined in whole IC model. The transformation of initial information into the form which would be suitable for IC designers is almost not included into IC design software packages therefore this exhausted work is usually done manually. An integrated circuit is constructed from a set of layers situated one above other and for each layer it is necessary to create its model. Each IC layer can be represented as a background with electric elements (transistors, resistors, etc.) connected by metal tracks.

There are known many papers devoted to analysis of IC images including overview paper[3] although most of them consider IC quality control problem [1, 8]. There are papers devoted to extraction of various IC or PCB elements like metal tracks, soldering points, etc.[5,7]. This task depends on structure and form of IC because of many types of IC being produced.

Reverse engineering for IC design requires extraction of all elements presented in IC and forming of IC vector description in a form suitable for applied system.

In this paper, we propose a method to automatically obtain a description of IC elements from grey-scale IC images. Main distinctions of the proposed method are stability in respect to noise and low error percentage. To speed-up the processing, the special algorithms for edge detection, image vectorisation and reconstruction of vector representation have been developed.

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2 Technology of IC image Processing

The nature of the task being investigated imposes some specific restrictions on the processing method: high level of noise in the image and possible corruption of IC surface during preparation procedure. Additional requirements are low percentage of errors in the output together with low computational time.

The technology is started from preparation of IC. The outer layer is acquired at first and further it is mechanically removed that gives an access to the next layer, etc. The removal is followed by further chemical preparation. It is repeated for all the layers of IC. The required IC layer is taken by IC acquiring system. The existed image objects have to be extracted, classified and represented in terms of IC design system (vertices of rectangles and polygons with their topological relationships).

Digital description of IC topology includes a vector description of borders of IC elements as well as their parameters and mutual relationship. To obtain it, the following technology was developed:(Fig.1). Detailed implementation of all technology stages is explained below.

Image Acquisition

The IC image is taken by a system containing microscope, videocamera, digitiser and movable basement to fix and to transport the IC before objective. An important step in image acquisition is choosing the optimal resolution to ensure a required quality of objects on the IC image. Small resolution brings big part of a layer to the single image, but small details are indistinguishable there. On the other hand, the IC layer is not flat: metal tracks are higher that background and complicated elements are higher than metal tracks. That is why very high resolution does not allow to simultaneously obtain clear-cut edges of metal tracks and other elements. The optimal resolution of

the system was chosen during experiments and is equal to 10 pixel/μm. Taking into account that obtained image has a size of 640x442 pixels, it is possible to acquire just small part of the IC layer at once. Therefore, whole IC layer is represented by a set of images acquired with overlapping in 10 pixels.

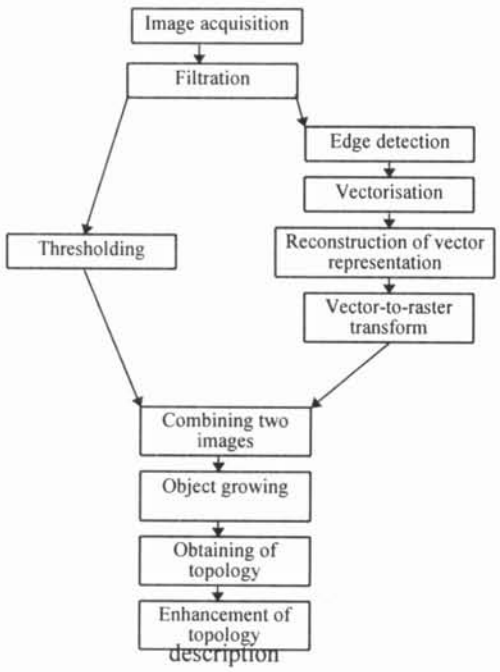

Fig.1. The technology of IC image processing.

At the first step image noise should be eliminated. An iterative 3x3 mean filter is applied three times to do it. An example of initial IC image is shown in Fig.2.

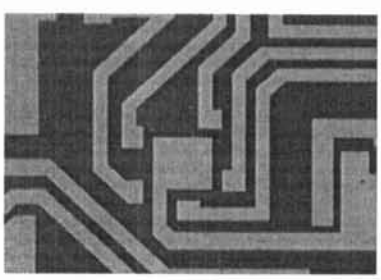

Fig.2. An initial IC image

Feature Extraction

Extraction of the IC topology from image processing point of view means that all IC elements must be extracted as correct geometric figures with straight borders, parallel opposite sides, etc. The most obvious solution of this task is to binarise the image with further border extraction, but high level of image noise does not allow to obtain a qualitative result. Moreover, even sophisticated local thresholding algorithms do not give desirable results.

Detail analysis of the image nature has shown, that edge detection methods can give better borders of IC elements, but no information about topological relationships between different IC elements could be obtained. To get the information about element borders and topological relationships between them, we propose to use edge detection and thresholding methods simultaneously. The edge detection method gives a precise border position, whereas the thresholding method produces information about topological relationships between IC elements.

a) Edge Detection

The edge type, which suits best to track borders we have, is a concave roof edge. Some experiments were performed to define the optimal number of masks as well as their configuration.

The optimal mask configurations are shown in Fig.3.

```
 1  ...  1  ...  1
 0  ...  0  ...  0
...  ...  ...  ...  ...
-2  ... -2  ... -2
...  ...  ...  ...  ...
 0  ...  0  ...  0
 1  ...  1  ...  1
```

Horizontal orientation

```
 1  0  ...  -2  ...  0  1
...  ...  ...  ...  ...  ...  ...
 1  0  ...  -2  ...  0  1
...  ...  ...  ...  ...  ...  ...
 1  0  ...  -2  ...  0  1
```

Vertical orientation

Fig.3. The optimal configurations of masks

To define the optimal scale of mask, its size was sequentially changed to 3,5,7 by zero rows adding or taking off. The optimal masks are shown in Fig.4.

```
 1  1  1
 0  0  0
-2 -2 -2
 0  0  0
 1  1  1
```

Horizontal orientation

```
 1  0  -2  0  1
 1  0  -2  0  1
 1  0  -2  0  1
```

Vertical orientation

Fig.4. Masks of operator for edge detection

An initial image was convolved with each mask and edge strength and direction were calculated for each pixel. The pixels, with edge strength being local maxima in the direction perpendicular to the edge

direction have been considered as the border ones. We need to use quite large masks (5x3 and 3x5) for edge detection due to noise presence. But these masks do not work well in the corners of IC elements, that is resulted in gaps in the corners. To remove the gaps, we use vector representation reconstruction stage described later. An example of IC image with detected edges is shown in Fig.5.

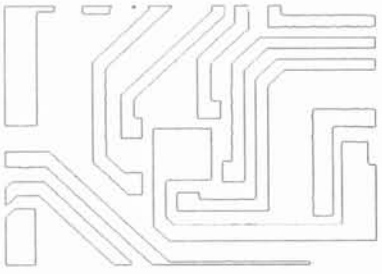

Fig.5 IC image with detected edges

b)Thresholding

To perform an image thresholding, we use a histogram-based method that allows to satisfactory separate an image into two classes: elements and background.

Vectorisation

To transform the detected edges into vector representation, we use fast vectorisation algorithm that was proposed by us in [6]. It is based on assumption that all element borders are represented as a set of straight lines. To extract straight lines, we use a notion of a primitive line (PL) that is a set of 4-neighbour pixels in a horizontal/vertical direction. PL has three possible orientations: horizontal, vertical and undetermined, which is used for PL with one-pixel length.

Generally, a straight line in a discrete image can be considered as formed by PLs with the same features (orientation, length, etc.). For extraction of strength lines it is necessary to find required sets of PLs among all PLs of the image.

To extract PLs, we use a binary image obtained by edge detection. The PL is vectorised by the contour line tracing and the following characteristics for any PL are calculated: orientation, length, the first and the last pixel co-ordinates, and direction to the next PL(NPL).

To join PLs into straight lines, we use a cluster analysis method. One cluster corresponds to one line segment. The new PL is joined to the cluster if the following conditions are satisfied: it is connected with cluster of the line already found, it has the same orientation, it has the same NPL direction and deviation of its length from average cluster length does not exceed given threshold (it was equal to three pixels in our case).

The line segments are described by end point co-ordinates.

Reconstruction of vector representation

The reconstruction is performed in two stages: (a) removal of gaps within line and (b) removal of gaps in corners.

a) Removal of Gaps Within Line

The structure of obtained vector representation is not suitable for IC reconstruction due to defects like local gaps. To remove a gap, we have to extract and to merge lines bounding it [6]. Special kind of data representation was developed to avoid multiple search of the line to be merged. Lines are divided into five groups in according to their orientation. First four groups are ranked by the parameters given in the *Table1*. Shown values correspond to cartesian coordinates of a line centre.

Table 1

Line group	*Parameter 1*	*Parameter 2*
Horizontal	y	x
Vertical	x	y
Diagonal	x-y	x+y
Anti-diagonal	x+y	x-y
Other	not processed	

At first, group items are ranked in accordance to *Parameter 1*. The second ranking stage is performed to distinguish different lines with the same value of *Parameter 1*. Such vector representation allows to easy perform reconstruction stages. No search is required to find neighbouring lines to merge them, because they are always situated at neighbouring positions in the vector representation.

b) Removal of Gaps in Corners

It is performed by growing all lines, obtained during the previous operation on definite length in both directions. Perpendicular lines are crossed removing a gap. The reconstructed vector representation is shown in Fig.6.

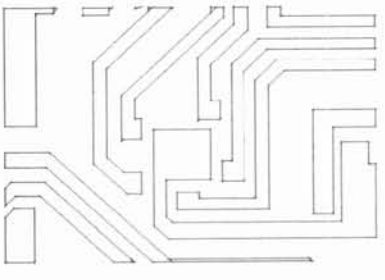

Fig.6. The reconstructed vector representation.

Vector-to-raster transform

To be able to combine the result of edge detection and the result of thresholding, we perform vector-to-raster transform for detected borders. It is performed by algorithm of Breesenham[4]. The detected edges are superimposed with the thresholded image and the resulting image contains information obtained after application of both methods.

Border analysis

Later on, areas of IC elements (obtained by thresholding) are grew to their true borders (obtained by edge detection). As a result, we obtain a binary image with black background and white elements having correct borders and true topological relationships.

Obtaining IC topology

To obtain IC topology, we trace border of each IC element and transform it into format of the existed applied system, which allows to analyse and to check the topology of an integrated circuit. Checking of IC parameters is simultaneously performed.

An example of an image with extracted topology is shown in Fig.7.

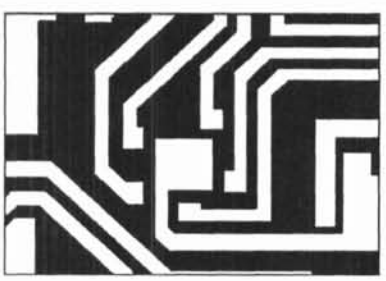

Fig.7. Image with extracted IC topology.

3 Experimental Results

The described technology has allowed to design the reliable system for IC topology extraction. The use of such a system allows to avoid most part of manual operations in the IC quality checking and reverse design applications. The developed system is used now to digitise IC in a company producing integrated circuits. Until now, it was used to digitise more than one thousand images.

During practical use of the system, it was found that there are small errors in processing IC elements having borders with constantly changing curvature. They are occur rarely, but the detected borders do not follow precisely the true borders.

Our technique can be extended to the images containing three or more classes of elements. An image is divided into small fragments, bounded by result of edge detection and for classification of them more advanced classificator can be used. The method of IC image processing with three classes (background and two classes of elements) is now under investigation.

Now we also investigate the use of a priori knowledge for increasing of extraction process reliability.

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