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VLSI Optimal Edge Detection Chip: Canny-Deriche Filter

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Abstract

This paper presents the design of an ASIC intended for optimal edge detection of blurred and noisy 2-D images. The chip has a parallel and pipelined architecture which processes any second order recursive filters. The architecture can be extended to process third order recursive filters also.

1 Introduction

Edge detectors are an essential part of many computer vision systems. Several methods have been proposed and most of them use local operators. For example, there are gradient operators and second-derivative operators followed respectively by threshold and zero crossing detections. Among these operators we find Robert, Sobel, Prewitt, Kirsh and Laplacien [1] which use 2-D convolution of the image with 2 × 2 or 3 × 3 windows. The performance of these operators deteriorates rapidly when they are used for blurred and noisy images.

New approaches were developed a couple of years ago to extract edges. They use the optimization of criteria which takes into consideration a predefined model of the edge. One of these approaches is Canny's optimal edge detector [2]. He defined a model of a step in white Gaussian noise and assumed that the detection was performed by convolving the model with a spatial antisymetric function which should give a good detection, good localisation and one response to one edge. Canny found an approximation of the optimal filter, the first derivative of a Gaussian, and he used it as a F.I.R filter (Finite Impulse Response).

The approach of Shen and Castan [4] is very close to Canny's algorithm but it uses only one criteria of optimization, which gives an exponential function. Deriche [3] found a new operator which performs better than Canny's operator :

$$f(x) = A.x.\overline{e}^{\alpha|x|} \tag{1}$$

It is implemented as 2-D second order Infinite Impulse Response (I.I.R) digital filters, and presents only one parameter, α. This parameter is adjusted to yield the desired location or signal to noise ratio.

A recent study in the University of Bourgogne [6] considers that the edge has an exponential model and not a step. This study led to a new operator which gives more performance than Deriche's operator. It is implemented with third order recursive filter.

The first part of this paper will develop the Deriche algorithm, the second part will describe a hardware implementation of the algorithm and the last part will present the architecture of the convolution unit.

2 The algorithm of Deriche

The Deriche algorithm consists of calculating the first directional derivates of the image pixels in the horizontal direction from the left to the right, then from the right to the left, using second order recursive filters, as is shown in the following equations:

$$X^+(i) = I(i-1)+2e^{-\alpha}X^+(i-1)-e^{-2\alpha}X^+(i-2) \tag{2}$$

for i=1...M

$$X^-(i) = I(i+1)+2e^{-\alpha}X^-(i+1)-e^{-2\alpha}X^-(i+2) \tag{3}$$

for i=M...1

$$S(i) = c_1[X^+(i) - X^-(i)] \quad \text{for} \quad i = 1...M \tag{4}$$

$$\text{with} \quad c_1 = -(1 - e^{-\alpha}) \tag{5}$$

I_i is an input pixel; M is the size of the ligne. The resulting image S is then filtered in the vertical direction from the top to the bottom, then from the bottom to the top as in the following equations:

$$\begin{aligned} R^+(i) = \; & K.S(i) + K.e^{-\alpha}(\alpha - 1)S(i-1) \\ & +2e^{-\alpha}R^+(i-1) - e^{-2\alpha}R^+(i-1) \\ & \text{for} \;\; i = 1....M \end{aligned} \tag{6}$$

$$\begin{aligned} R^-(i) = \; & k.e^{-\alpha}(\alpha + 1).S(i+1) - e^{-2\alpha}.S(i+2) \\ & +2e^{-\alpha}.R^-(i+1) - e^{-2\alpha}.R^-(i+2) \\ & \text{for} \;\; i = M....1 \end{aligned} \tag{7}$$

$$R(i) = R^+(i) + R^-(i) \;\; \text{for} \;\; i = 1....M \tag{8}$$

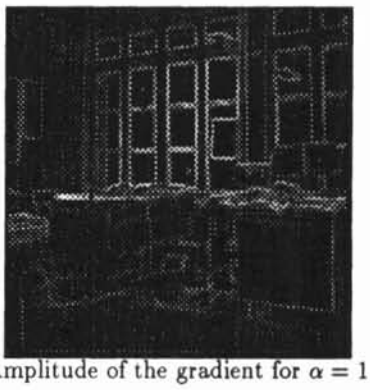
$$\text{with} \;\; K = \frac{(1 - e^{-\alpha})^2}{1 + 2\alpha.e^{-\alpha} - e^{-2\alpha}} \tag{9}$$

The same technique can be applied to obtain the vertical gradient. The size of the filter can be varied by simply changing the value of the parameter α.
The recursive nature of the filtering operations leads to a substantial saving in computational effort (14 multiplications and 11 additions for each pixel). The C.P.U time to process the two gradients of the 256 × 256 8-bit image on Apollo DN3000 (1 MIPS) workstation is about 50 s. In order to meet image analysis requirements in terms of processing speed and computing capacities, we have developed an integrated circuit which needs only 25 ns to compute the two gradients. Figure 1 shows the initial image, the amplitude of the gradient and the edge image calculated using the algorithm of Deriche for $\alpha = 1$ with fixed point representation (coefficients are represented by 8 bits and the computations by 16 bits).

3 Functional description of the chip

Most of the edge detection circuit use local operators which need a 2-D convolvor. For example, the CC33 [7] is a 3 × 3 convolvor extended to 15 × 15. The coefficients of the window are dynamically programmed. The chip area is 56 mm^2 in 1.3 μm HCOMS technology with an 84PGA package.
INP20 [8] is a monochip for image analysis, which can handle convolutions with Kernels up to 20 × 20 at video rates, as well as 12-bit grey level morphology (up to 20 × 20) or all usual image operations (accumulation, projection, inter-image,etc.). The chip area is 80 mm^2 in 2μm CMOS technology and encapsulated in an 84 pin package.
The circuit described in [9] is a real time image processing microsystem which detects defects in manufacturing products. The analysis method is based on the

Initial image.



Amplitude of the gradient for $\alpha = 1$

Edge image with hysterisis threshold

Figure 1: Edge detection using the alogorithm of Deriche

algorithm of Robert to select the information related to the structure of the objects present in the image. The edge calculation function has been integrated in a standard cell circuit, using the CMOS 1.5 μm process and the chip area is 36 mm^2.
The DMA machine [10] (Depth and Motion Analysis) has two applications:

- The recognition, localization and handling of parts for an industrial assembly cell.
- The navigation and exploration of a mobile robot in an office environment .

This machine has one board for edge detection using the technique of Deriche, but unfortunately the recursive filters have not been put in hardware for technological reasons. L64240 FIR filters from LSI logic are used instead of the recursive filters.
The chip that we will introduce in the next paragraph presents the design of the algorithm of Deriche using IIR filters. The chip can also compute other algorithms such as Shen algorithm [4] and algorithms to extract ridge-lines and step [5]. The chip is programmed using a PC board to compute the horizontal and the vertical gradients, and the magnitude and the threshold are done by software.

4 The architecture of the chip

Our chip requires the processing of only two memory planes: one for the initial image and the other for the gradient image. The chip has a pipelined and parallel architecture which allows real time processing. Figure 2 shows a bloc diagram of the chip which consist of the following units: the programming unit, the convolution unit, the LIFO memory, the counters and the state machine.

4.1 The architecture of the convolution unit

The convolution unit computes a digital convolution of second order recursive filters of the type:

$$X_i = a_0 I_i + a_1 I_{i-1} + b_1 X_{i-1} + b_2 X_{i-2} \qquad (10)$$

The classical structure [11] consists of using 4 multiplications, 2 delays and 3 adders. This structure (figure 3) is very slow because the time processing needed is one multiplication and two adders.

A structure developed in [13] uses pipelined multipliers in order to reduce the time processing, but unfortunately it needs three times more multipliers and adders to have the real time processing.

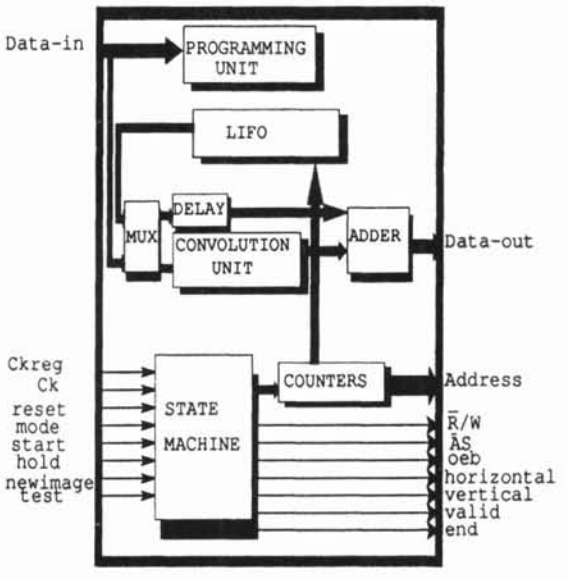


Figure 2: Functionnal block of the architecture

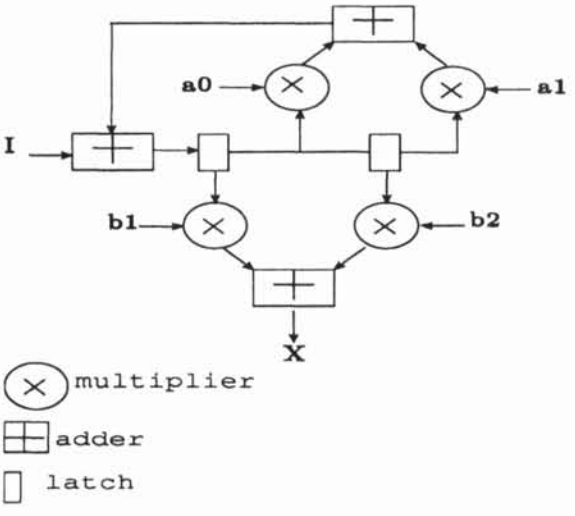


Figure 3: Classical architecture of the convolver

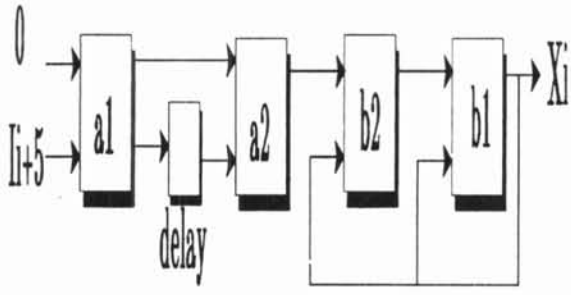


Figure 4: Architecture of the convolution unit

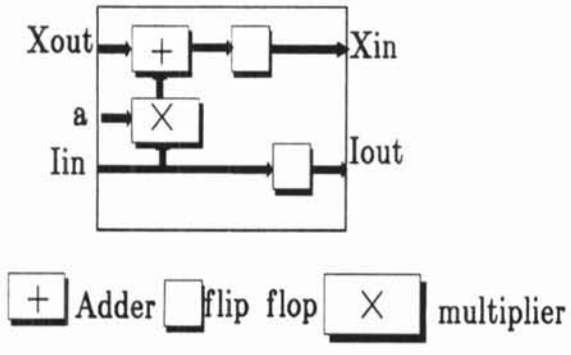


Figure 5: Basic cell of the convolution unit

The structure which we propose has a systolic architecture [12]. It needs only 3 adders and 4 multipliers and the time processing is one multiplication and one addition. The convolution unit consists of 4 identical stages. Each one has one 16-bit adder, one 8-bit multiplier, one 16-bit register and one 8-bit register as is shown in figures 4 and 5.

This architecture can be extended in order to compute third order recursive filter by adding two more stages without changing the time processing. The chip is designed in 1.5 μ CMOS technology using COMPASS. The chip area is 66.5 mm^2, the number of transistors is about 182 000 and the power consumption is 750 mW.

5 Conclusion

The chip that we have presented is designed to perform optimal edge detection for blurred and noisy images. The chip implements second order IIR filters (algorithm of Deriche) and can be programmed to compute first order IIR filters and can be extended to third order IIR filters.

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