AN IMAGE SENSOR FOR SHEET-OF-LIGHT RANGE IMAGING

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ABSTRACT

Range image acquisition can be made in many different ways. In this paper the range data are acquired by using a sheet-of-light to illuminate the scene [2], [3]. Our image sensor design incorporates the concept of Near-Sensor Image Processing (NSIP) where the individual sensor operation is an integrated part of the signal processing algorithm [1].

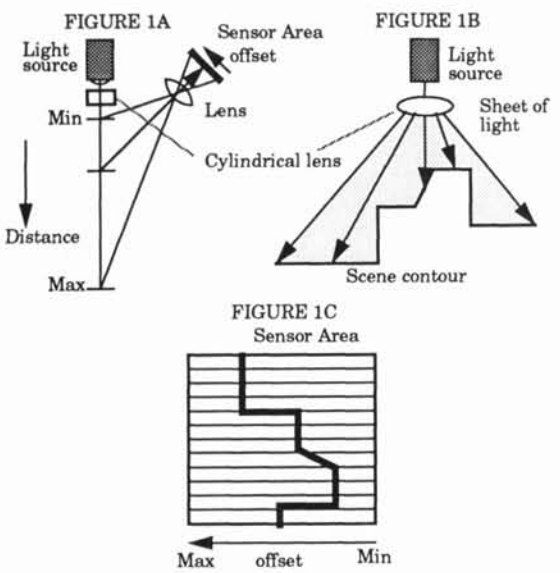
This architecture can provide range images with very high frame rates. The limit is set by the integration time in the sensor, and we believe that a full range image can be captured in 6.5 ms. The NSIP design is automatically adaptive to different light intensities since the utilized integration time for each cell depends on the incoming light. There is no transfer of analog data; each sensor cell output is binary and thus there is no signal degradation in the image readout. Auxilary logic is incorporated to automatically obtain sub-pixel accuracy and an error indicating bit to indicate low confidence range values. Concurrent with the range image, the chip can also produce a grey level reflectance image.

SHEET-OF-LIGHT RANGE IMAGING

In a sheet-of-light system range data is acquired with triangulation, see Figure 1A. The offset position of the reflected light on the sensor depends on the distance from the light source to the object. To make a sheet-of-light the laser light is passing a cylindrical lens, see Figure 1A-B. For each position of the sheet-of-light a one dimensional range image is acquired, see Figure 1C. Two dimensional images can be obtained in at least three ways: by moving the apparatus over a static scene (in a road survey vehicle [4]), by moving the scene (conveyor belt [5]) or by sweeping the sheet-of-light over the scene [10]. In the two first cases the distance can be computed from the offset position in each row with a simple lookup table. In the latter case the direction of the emitted sheet-of-light changes so that a full triangulation computation has to be made to obtain the distance to the objects in the image.

In any case, for each illumination position (and sensor integration) as a first computational step the output from the 2D image sensor should be reduced to a 1D-array of offset values.

FIGURE 1.



A range camera using sheet-of-light. Figure 1A shows the illumination with the sheet-of-light perpendicular, Figure 1B parallel to the plane of the paper. Figure 1C shows a snapshot of the sensor area.

THE SENSOR ARCHITECTURE

In the sensor the photo diode and a comparator is used together to obtain a digital, binary output, see Figure 2A. The incoming light will induce a current, proportional to the intensity, through the precharged photo diode. The time from the precharge of the diode to the time the diode voltage passes the reference voltage of the comparator is inversely proportional to the light intensity, see Figure 2B.

FIGURE 2.

FIGURE 2A

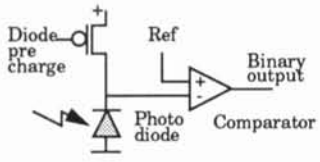
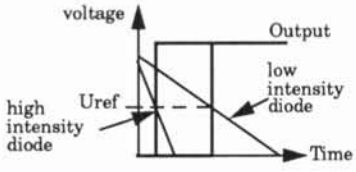


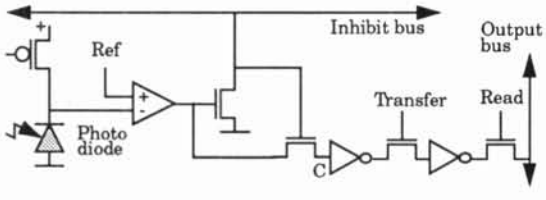
FIGURE 2B



The NSIP design. Figure 2a show the schematic of the diode and comparator. Figure 2b show the output as a function of time and intensity. The steep line represents high light intensity, and the shallow line low intensity.

The design of a complete individual sensor cell can be seen in Figure 3. (Please note that this is a principal sketch and not a complete circuit drawing.) The sensor area consists of a two-dimensional array of sensor cells which are interconnected via the inhibit and output buses. The integration starts after the photo diode has been precharged. As mentioned, it is then discharged proportionally to the incoming light intensity. When the first photo diode in the row is discharged to the point where the value goes below the reference voltage the comparator switches, and the inhibit bus goes low from its precharged high. Thus, all sensors in the row are forced to freeze their outputs at C. Interpreted as binary signals these values are all zero except for the cell with the highest intensity (and which took command over the inhibit bus). When the transfer transistors are enabled the output data are moved from the first inverter to the second, and a new integration can begin in the photo diodes. The readout is then made one row at a time concurrently with the next integration in the sensors.

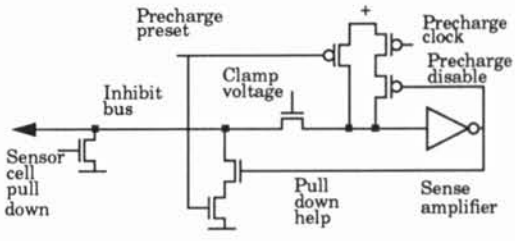
FIGURE 3.



A complete single cell in the sensor array. The inhibit bus is precharged high.

The inhibit bus must be designed to switch very fast when one cell tries to pull it down. To do this we employ a memory-readout design at the edge of the bus, see Figure 4. The clamp transistor will amplify any charge leakage from the bus and the sense amplifier will detect this. When a change is detected the change is fed back and used to help pull the bus down faster. The pull down help transistors can be made larger than the pull down transistors in the cells, and drivers can be used to increase the switching speed.

FIGURE 4.

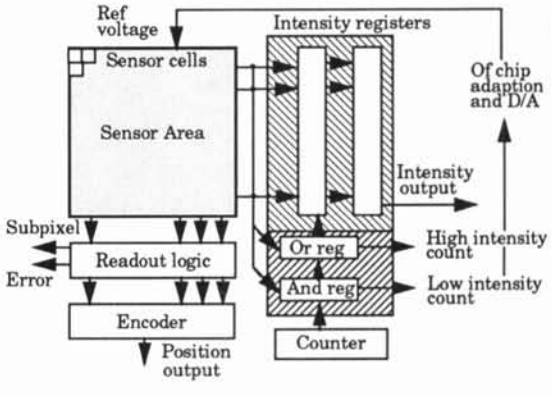


The inhibit bus pul-down design. The design is made as a memory readout bus.

GLOBAL ARCHITECTURE

The global architecture is showed in Figure 5. From the 2D-array of sensors, binary data is read one row at a time, and the binary code of the position of the single *one* is obtained with an *encoder*. We also has to handle the case when more than one sensor position is set to one, and this is done in the *readout logic*, which outputs a single *one*, a *sub-pixel* bit and an *error* indicator to be described below.

FIGURE 5.



The global architecture. The area marked by down-slanting lines is the intensity image circuit, and the area marked by up-slanting lines is the circuits for adaption to different light levels.

The time from the start of the integration to the activation of the inhibit bus is inversely proportional to the light intensity in the maximum intensity position. This intensity depends on the reflectance (brightness) of the surface swept by the sheet-of-light. A full reflectance map, an intensity image, can be obtained as follows by circuitry in the area which is marked by down-slanting lines in Figure 5. A *counter* is started when the sensors are activated, and when an inhibit bus is triggered the corresponding register is loaded with the counter value. These registers are then addressed simultaneously with the row output so that both the position and its intensity value are output concurrently. To be able to use this design concurrently with the integration, the registers have to be doubled so that one set of registers can be loaded from the inhibit bus while the other set is used for output.

Hardware to faciliate automatic adaption of the reference voltage (integration time) is also incorporated in the design shown in the area which is marked by up-slanting lines in Figure 5. This adaption is based on the integration times for the first and last row to reach the reference voltage, and they are computed by taking a *Global Or* and *Global And* on the inhibit buses. The *Or* function will react for the first transition, the *And* function for the last. To get the best signal to noise ratio the integration times should be as long as possible. This means that the reference voltage should be as low as possible without missing a row with significant reflected light.

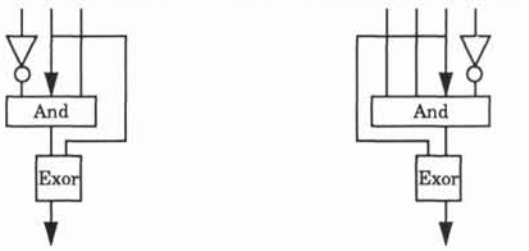
THE READOUT LOGIC

The sensor rows are designed so that the resulting binary vectors only contain a single one which corresponds to the position of the maximum intensity. However, if several ones are found the correct output should be interpolated from the vector.

If the output contains one consecutive row of ones the light sheet is unfocused on the array so that no sharp maximum is found and the correct output ought to be the centroid value. Ideally, the vector is expected to have one or maybe two ones if the light is focused. We have chosen to accept up to three ones as a correct answer but if more than three consecutive ones are found an error will be indicated in the output.

The first operation on the output vector is connectivity preserving erosion from the left and the right, done with the logic seen in Figure 6. This stage erodes two and three consecutive *ones* to a single *one*. If only two pixel are set a special ripple chain is used to output a half-pixel position bit which is used as the least significant bit in the position vector.

FIGURE 6.

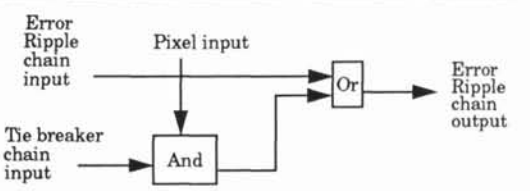


Connectivity preserving erosion from the left and from the right. Erosion from the right is only performed if more than two consecutive ones are found.

If the readout contains several ones which are not consecutive there are mainly two reasons. The first is that the light is reflected from an edge so that part of the light come from the closest area connected to the edge and part come from the farthest area. The other reason for two disparate ones is shadowing, in which case the only light which reach the sensor row is background light. If this occurs an error will be indicated in the output.

The error indicator logic seen in Figure 7 checks if there is more than one bit left after the erosion stage, in which case the error bit will be set by the logic. Thus, the error bit will be set if there was more than three consecutive ones or more than one group of ones in the read-out vector.

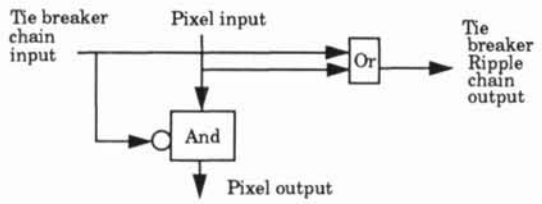
FIGURE 7.



Error indicator logic. The output is one if there is more than one bit of output after the erosion stage.

Since the encoder only accepts one bit set high a special tie-breaker ripple chain is used to block all but the leftmost one found after the erosion stage, see Figure 8. That several ones might be blocked does not affect the sensor output as this is detected in the error indicator.

FIGURE 8.



The tie-breaker ripple chain. A pixel output can only be one if no previous pixel have been one.

CONCLUSIONS

We have presented a high speed solution for range imaging with sheet-of-light. The key point is the row-wise max detector. We believe this solution is much simpler than other designs for instance the one suggested by T. Kanade [7].

The architecture gives half-pixel accuracy and an error value to indicate when range data is uncertain. Results of the error filtering technique is reported in [11]. This error filtering technique is unique and cannot be found in analog PSD based techniques such as the one proposed by Araki et. al [10]. An intensity image of the scene can be produced concurrently with the range data.

We estimate that, using a CMOS process with $\lambda = 0.8\ \mu m$, 128x128 cells of the type shown in Figure 3 should fit on a 10x10mm chip. An image integration time of 50 μs gives a row readout frequency of 2.5 MHz. If a full range image is assumed to consist of 128x128 data points (rangels) these should be possible to acquire in 6.5 ms.

Our implementation efforts will focus on the design and simulation of the sensor circuitry, especially the comparator, the size of which should be minimized, and the inhibit bus, which must switch very fast. Naturally, the area percentage of the sensor diodes must be kept as large as possible, but the effective aperture can be increased by using binary optics [8].

A more complete description of the above described design, including variations and comparisons with other architectures is found in [6].

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