IAPR Workshop on CV - Special Hardware and Industrial Applications OCT.12-14, 1988, Tokyo

HIGH SPEED 32 BITS IMAGE PROCESSOR SYSTEM DSPT 9506

Tsukasa Kobayashi, Eiji Osaki, Kohei Horiguchi and Hiroshi Yahiro

Toshiba Corporation
1 Komukai, Toshiba-cho, Saiwai-ku, Kawasaki, Japan

ABSTRACT

There is growing need recently for high-speed digital image processing in various fields. High-speed and flexible 32-Bit Image Processor Boards have been newly developed for such need.

These are compatible with Multibus (IEEE-796) or VME bus (IEEE-1014) and mount a large memory and image processor VLSI T9506. These processor boards are capable of carrying out 1,024-point complex FFT in 2.0 msec and provide many functions for image and/or signal processing. This paper will describe overview of these boards and some application as well as associated softwares.

1. INTRODUCTION

The demand for high speed and compact image processor system has been increased in remote sensing, medical imaging, printing and publishing and machine vision.

At the same time, high-performance VLSIs are drawing attention as devices for dedicated application in the image and digital data processing fields.

As one of such devices, the T9506 is characterized as high-speed and high-precision performance and provides unique capability of multi-functions for processing imagery and signals in various ways by simply re-writing stored program.

Full advantage can be taken of such characteristics in the application of the T9506 not only to image processing but also to analyzing vibration, shock and accoustic phenomenon.

The T9506 was mounted on the processor board compatible with Multibus (IEEE-796 bus). The processor board was then incorporated into a compact, high-speed, high-performance image processor unit, DSPT 9506, with low cost.

In addition, we have developed new processor board compatible with VME bus (IEEE-1014) by using gate-array of peripheral circuit on compact circuit board.

The hardware and software of these Multibus and VME bus compatible processor boards, some example of system configuration and its applications are described in this paer.

2. MULTIBUS PROCESSOR BOARD

Multibus processor board is a image/signal processor board mounting high-speed image processor VLSI T9506, Multibus (IEEE-796) interface and high-speed data bus for operating a large amount of data. Fig. 1 indicates block diagram of the Multibus processor board.

The Multibus processor board consists of T9506 as a core, data memory, control bus interface, high-speed data bus interface and peripheral circuit around T9506.

The image and signal are processed between the T9506 and the data memory (512×512×8 bits×3 channels) with 10 MHz clocks. The structure of data memory is changable to 256×256×32 bit for 32 bit processing.

Fig. 2 indicates external view of Multibus processor board. Table 1 shows the typical board specifications and the processing speed for major functions.

The feature of Multibus processor board is characterized as follows:

(1) High-speed image and signal processing are possible by using T9506 and high-speed SRAM (10 MHz clock) on this processor board.

(2) By re-writing the program stored in the T9506, various kinds of imagery and signal processings are achievable.

(3) Software-overhead of host CPU are decreased by auto-loader which consists of IC memory (that can hold many micro-programs) and associated circuitry (that can transfer the micro-programs to T9506) on the processor board.

(4) With a high-speed data bus interface (8 bits × 3 channels), the board permits the data transfer at a maximum rate of 10 MBPS so that high-performance measurement system could be configured.

(5) Direct interface with user system having the multibus is capable because the control bus interface is connectable to the multibus.

3. VME PROCESSOR BOARD

The application of gate-array has led to reduction in the size of the VME processor board and to increasing the board performance.

VME bus is suitable for image processing which uses a large amount of data because it has 4 GByte memory area and 32 bit data length.

The VME processor board is characterized as follows in addition to the same characteristics as those of Multibus processor board:

(1) Data memory is 512 x 512 x 32 bits x 3 channels, changable to 1,024 x 1,024 x 8 bits x 3 channels.

(2) Direct memory access to data memory from host CPU or VME bus is possible because each data memory is assigned on the VME bus area.

(3) Many micro-programs up to 80 can be kept on the RAM (auto-loader) because its capability is four-times larger (32 KWord) than the RAM on Multibus processor boards (8 KWord).

(4) High-speed data bus can transfer data at 40 MBPS and has 32 bit data length.

Fig. 3 indicates block diagram of the VME processor boards. Fig. 4 shows external view of the board and Fig. 5 shows also external view of the newly developed gate-array.

The size of the VME processor board is double-height (single board set contains linked two boards) by using memory-module and two types of the gate-arrays.

Each gate-array consists of 3,000 GATE or 2,000 GATE respectively and contains data control circuit, autoloader control circuit and high-speed data bus circuit. Each gate-array is packed in 160 PIN flat-package or 120 PIN flat-package.

Table 2 shows a major specification of the VME processor board.

4. EXAMPLE OF SYSTEM CONFIGURATION

(1) PC based image processor system

We have developed a compact and high-performance PC based image processor system which consists of a commercially available personal computer and a processor unit which includes the Multibus processor board with frame memory board, camera interface board, monitor interface board and A/D converter board as options.

Either Toshiba PASOPIA-1600 or J-3100 (T-3100 in US market) or IBM PC/AT is connectable, as host CPU, to this processor unit.

Many applications are possible to Remote Sensing, Medical Imaging, Printing & Publishing and Machine Vision with this processor system.

Fig. 6 shows external view of the PC based image processor system.

(2) EWS image processor system.

Fig. 7 shows an example of EWS image processor system which consists of the VME processor board and the frame memory board.

Toshiba's EWS AS3000 is used for this system as host computer.

This processor board can be inserted into expantion slots of the AS3000 via tripple-height converter board because AS3000 has the VME bus as control bus.

Newly developed frame memory is used for storing data. The memory has 8 MBytes capacity and an interface between high-speed data bus and VME bus. Table 3 indicates the system performance.

5. SOFTWARE

Software for the PC based Image Processor system is constracted by micro-codes, driver, subroutine-library and command-library.

The micro-code is transferred to the program memory in the T9506 for a certain operation.

The driver controls each function within the board and is described in assembler language.

The subroutine library and the command library are adequate combinations of the micro-codes and the drivers for image or signal processing. These libraries are described in FORTRAN and C language.

The MS-DOS is selected as the Operating System.

On the other hand, the software for the EWS image processor system consists of image processing library, DSP control program (DCP) and DSP driver. These softwares were developed on the AS3000. Operating System is UNIX.

The image processing library or DCP is usable by C language or FORTRAN and easy to be emulated, to other UNIX machine since they are described by C language.

Table 4 shows the usable micro-programs on these software. Every basic image or signal processing is possible by combination of the software element and therefore it is easy to design various application programs.

6. APPLICATION OF DSPT9506

The system which utilizes the Multibus processor board or the VME processor board is applicable to many kinds of field because they have high-speed performance and multi-functions.

Table 5 shows the application of the DSPT9506.

7. CONCLUSION

We have developed DSPT9506- "the Multibus processor board" and "the VME processor board" as well as software and confirmed the performance as the personal computer based image processor system and the EWS AS3000 system.

Intended high level of performance was verified with there systems in low cost.

Further application of the boards for extensive-multi-processor system is under way.

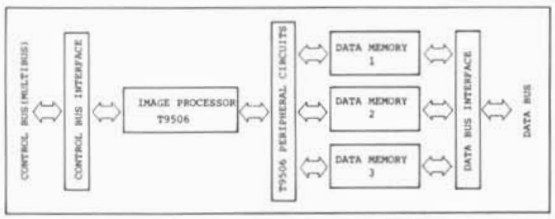

Fig. 1 Fundamental Schematic Diagram of Multibus Processor Board

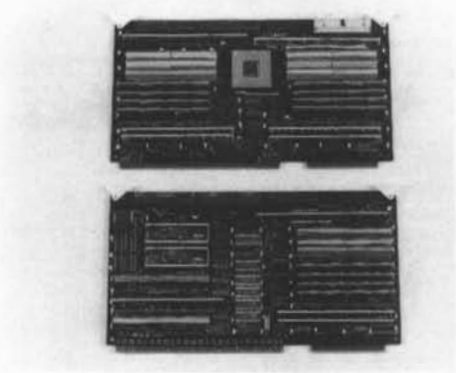

Fig. 2 External Views of Multibus Processor Board

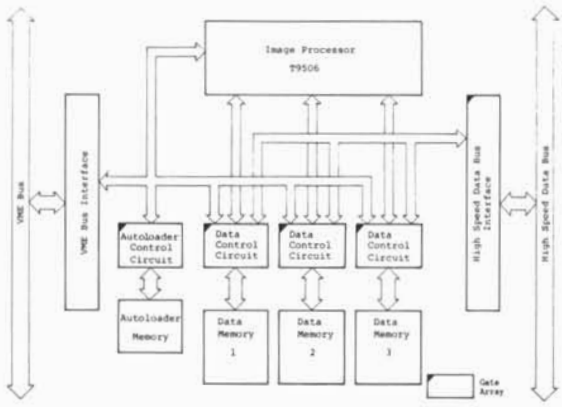

Fig. 3 Fundamental Schematic Diagram of VME Processor Board

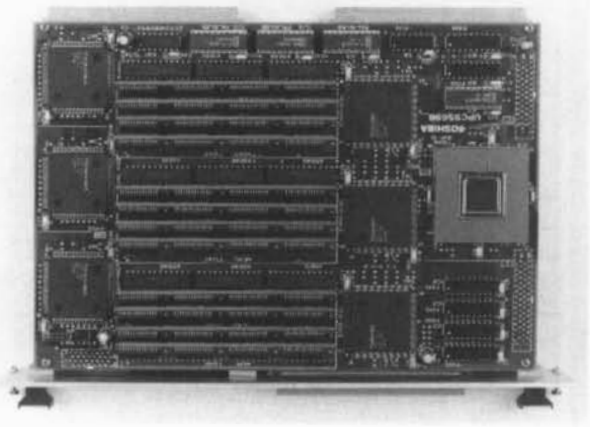

Fig. 4 External Views of VME Processor Board

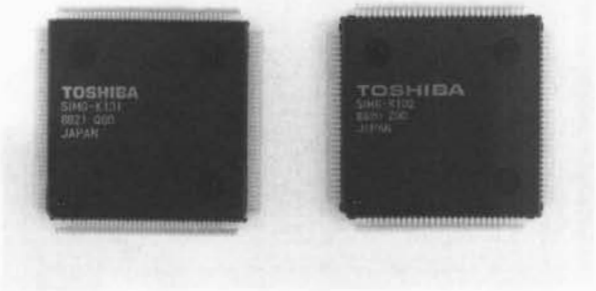

Fig. 5 External Views of Gate Array

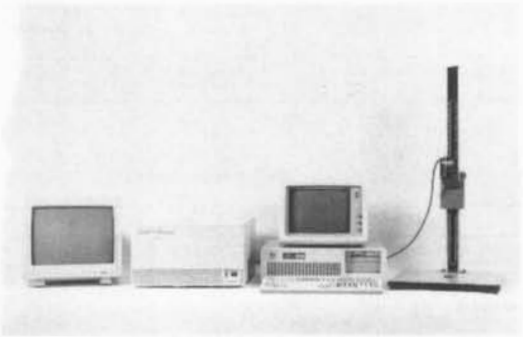

Fig. 6 External View of PC-based Image Processor System

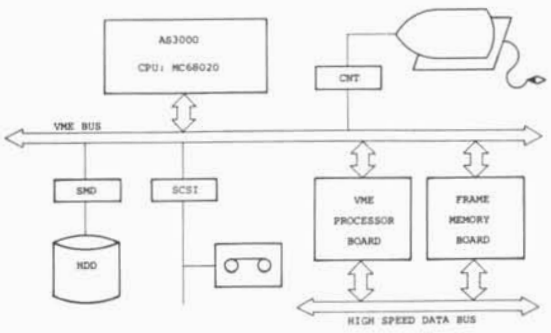

Fig. 7 Example of EWS Image Processor System

Table 1 Multibus Processor Board Major Specifications

ITEMS	SPECIFICATIONS
CONTROL BUS INTERFACE	Compatible with multibus (IEEE 796)
IMAGE MEMORY	512 × 512 × 8bits × 3chs.
CLOCK	10 MHz
BOARD SIZE	12 in. × 6.75 in. (2 boards for multibus)
NUMBER OF T9506	One chip
POWER SUPPLY	+5V only

FUNCTIONS	PROCESSING SPEED
FFT	2.0msec./1024 points, complex
SPATIAL FILTERING	1.0μsec./pixel (@3×3 mask)
AFFINE TRANSFORMATION	400nsec./pixel
HISTOGRAM	700nsec./pixel
MULTIPLICATION, ADDITION SUBTRACTION	100nsec./term (@64bit sum)
3×3 CONVOLUTION FOR 512×512 PIXEL IMAGES	262msec.

Table 2 VME Processor Board Major Specifications

ITEMS	SPECIFICATIONS
CONTROL BUS INTERFACE	Compatible with VME bus (IEEE 1014)
IMAGE MEMORY	512×512×32 bits × 3chs. or 1,024×1,024×8 bits × 3chs. , mapped on VME bus
CLOCK	10 MHz
BOARD SIZE	233.35mm × 160mm VME double-high-board × 1
NUMBER OF T9506	One chip
AUTOLOADER	32KWord, possible to keep many microprograms up to 80, continuous operation is available
HIGH-SPEED DATA BUS	32 bits Bus × 1 40MByte/sec

Table 3 System Performance

ITEMS	IMAGE SIZE	PROCESSING TIME	NOTES
AFFINE TRANSFORMATION	512×512	157.5 msec	Bi-Linear
SPATIAL FILTERING	512×512	315.0 msec	3×3 CONVOLUTION
INTER-PIXEL OPERATION (+, -, ×)	512×512	105.0 msec	
2 DIMENSIONAL FFT	512×512	1.3 sec	
	1,024×1,024	5.5 sec	

* at the case of frame memory I/O

Table 4 MICROPROGRAM MENU

		PROCESSING	NOTES
IMAGE PROCESSING	1	AFFINE TRANSFORMATION	Four-point interporation
	2	GRAY LEVEL TRANSFORMATION	Table look-up
	3	HISTOGRAM	
	4	SPATIAL FILTERING	Table size: 256×256 (max.)
PIXEL (DATA) PROCESSING	5	INTER-PIXEL ARITHMETIC OPERATION	Approx. 1.9 sec. for inter-pixel division of 512×512 pixels
	6	INTER-PIXEL LOGIC OPERATION	Inter-pixel AND, OR, XOR and INV operation
	7	ARITHMETIC OPERATION BETWEEN PIXEL AND CONSTANT	
	8	AVERAGE AND VARIANCE	
FREQUENCY DOMAIN PROCESSING	9	FFT/IFFT (COMPLEX NUMBER)	Number of data is the power of 2.
	10	FFT/IFFT (REAL NUMBER)	(Number of data = 2^n)
	11	COMPLEX NUMBER OPERATION	Operation between complex and conjugate
	12	CORRELATION OPERATION	
	13	CIRCULAR SHIFT	
OTHER PROCESSING	14	BIT OPERATION	Barrel shift and bit rotation
	15	RANGE CELL MIGRATION	Rearrange data on quadratic curve to one dimensional array
	16	SUM OF SQUARES OF COMPLEX NUMBER	
	17	MATRIX OPERATION	
	18	MEMORY CLEAR	
	19	MAXIMUM LIKELIHOOD CLASSIFICATION	

Table 5 APPLICATION FIELDS

	FIELDS	APPLICATION EXAMPLE
FFT APPLICATION	GENERAL	Spectrum Analysis
	COMMUNICATION, DATA STORAGE	Digital Filter, Data Compression
	STRUCTURE, MACHINE	Vibration Analysis, Impact Analysis
	ACOUSTICS	Sound Analysis, Voice Analysis
	IMAGE PROCESSING	Image Restoration, Spatial Frequency Analysis, Detection of Difference, Regular Noise Elimination, Synthetic Aperture Radar Image Reconstruction, CT Image Reconstruction
IMAGE PROCESSING APPLICATION	MEDICAL DIAGNOSIS, REMOTE SENSING	Geometric Correction, Noise Elimination, Gray Level Transform, Feature Emphasis, Classification (MLH)
	MACHINE VISION	Positioning, Image Measurement, Appearance Inspection, Pattern Recognition
	OFFICE AUTOMATION	Copy Machine, Others
	BROAD CASTING, PRINT	Commercial, Animation, Others
	OTHERS	Difference-detection of Ground·House, Image Processing of Telescope, Microscope