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A PROCESSOR ARCHITECTURE FOR DISCRETE WAVELET TRANSFORM PROCESSING OF GRAY LEVEL IMAGE

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Abstract

This paper presents a novel architecture for discrete wavelet transform processing of gray level image. From several processor-time allocation scheme we found a quite optimal one that efficiently use the available processor-time slots. The algorithm is then mapped into an array architecture . The resulted architecture needs less processing elements than conventional architecture and has a simple control scheme, thus reduces complexity and space requirements in hardware implementation .

1. INTRODUCTION

Discrete wavelet transform (DWT) is a very suitable tool for image anaysis particulary for image compression . The problem remains to be solved is to perform real-time computation of the transform in an efficient low-cost way . This paper describes an array architecture for discrete wavelet transform processing of gray level image . The wavelet that we actually used in our architecture is Daubechies wavelet [1] with 4 coefficient , but the architecture can be easily modified to implement other wavelets , because of the generality of the algorithm that is used to derive the architecture. In addition to its real time processing capability , the new architecture use PE more efficiently than other conventional architectures so it can be implemented in a smaller hardware system.

2. NEW INTERPRETATION OF DWT'S ALGORITHM

Multiresolution image decomposition by wavelet transform is a recursive process of single resolution (single stage) image decomposition.

In each stage of decomposition process , input image is decompose to four subimages : one low resolution subimage and three detail subimages of different orientation [2] . These subimages are produced by independent processes that can be performed concurrently . Single stage image decomposition algorithm is given by :

for I_n compute
{
$O_0 = HH$ ** I ;
$O_H = HG$ ** I ;
$O_V = GH$ ** I ;
$O_D = GG$ ** I ;
}
where :

$$(FF ** I)_{m,n} = \sum_k \sum_l ff_{2m-k,2n-l} i_{k,l}$$

In : image of resolution n
(I_0 : original image)

Conventional interpretation sees each line in the algorithm equation above as filtering process that is followed by downsampling [2][3]. If this scheme is used in the hardware array structure to solve real-time transformation, every processing element in the architecture will have to spent all its time slots to compute transform coefficients . To compute four kinds of coefficients ,it needs four similar structures.Moreover, to obtain all coefficients of all resolution involved in multiresolution decomposition we have to

feed back the result of single stage process into the process again several times or cascading n similar structures in a pipeline.

Ironically, only 1/4 of the outputs will be preserved (i.e. one column out of two columns in the same row, and one row out of two rows) while the rest of the output is thrown away .

If we could manage a scheme such that the processing elements didn't have to compute unused coefficients , then we have 3(three) spare processor-time slots of every four processor time slots. These three slots can be used to compute other wavelet coefficients . The utilization of the spare slots will increase efficiency and open the possibility of reducing the number of processing elements required and or processing time.

There are several computation scheme in utilizing the slots (including the spare slots) . Recall the fact that we have to compute coefficients of different orientation (i.e. HH, HG , GH, GG) of different resolution.Assume that data come in raster scan form. Different approaches have been taken in different architectures to compute the coefficients.

One of the popular approach is by utilizing the interleaved slots to compute coefficient samples of different resolution in the same orientation[4][5] .Coefficients from different orientations are computed in separated structures. It is hoped that this scheme would lead to the optimal 2D decomposer architecture just like its 1D architecture . Unfortunately , the 2D case is not as simple as 1D case . We found that this approach cannot make use all of the spare slots (there are vacant spaces; most of them are located in the beginning of the sequence) and needs a complicated control scheme.

To avoid these difficulties, we take a different scheme in computing . In our approach coefficient samples of different orientation of the same resolution are computed in the same array on different interleaved time slots. The advantages of this approach are better slots utilization and simpler control scheme . The disadvantage is that we have to provide several similar array structure for multiresolution process.

Inappropriate interpretation is the key factor behind conventional architectures inefficiency , therefore, finding an appropriate interpretation of the algorithm is very crucial. We found that we didn't have to interprete the equations but instead mapped them directly into a dependence graph . The dependence graph was translated then into a signal flow graph with direct N dimension to 1 dimension mapping method . Finally, the signal flow graph was transformed into semi-systolic architecture. Using this method we obtained an array architecture that optimized real-time computing capability with minimum array dimension . The array performs necessary computations only , so it can compute all wavelet coefficients by using interleaved time slots.

3. PROCESSOR ARCHITECTURE

The proposed architecture is shown in figure 1. Data flow in the line delay in a raster mode . To synchronize the insertion , computation control unit (CCU) and external unit communicate through BUSY, REQUEST and REPLY line.

Line delays provide five consecutive row of image data to data sequence controller . Data sequence controller selects inputs from five input lines and passes them to four demultiplexers which controls insertion of data samples to appropriate input lines at correct time according to computation schedule.

Each PE multiply the input data with one of four coefficient that is selected by CSEL signals issued by the CCU . The coefficients selection time-table for one particular PE of a row array is shown in the row array internal architecture (figure 2). The result is passed to the next PE on the arrival of clock event (CLK) ; at the end of array the result flow out . Outputs from all row arrays are added together to obtain the complete result.

During the insertion of samples of even line, all row arrays compute HH and HG (orientation) samples interleavely and

during odd line input insertion , they compute GH and GG samples.

Because the input sequence (raster scan) flows continuously from line to line and from frame to frame, we have to provide control signals (GRST, P3C,P1C,P0MC ,P00SC,P01SC,P02SC and P03SC) so the array will always give the correct result. With this arrangement the array can do real-time processing of data in raster scan form.

4. SIMULATION AND CURRENT DEVELOPMENT PHASE

We have developed a VHDL model for our proposed architecture and simulated it on QuickSimII simulator. The simulation showed satisfactory results and gave functional verification for the architecture. The current development phase of this project is the implementation of the array architecture and computation control unit in a fast prototyping system using 5 (four) Field Programmable Gate Arrays (FPGAs) with 10,000 gates equivalent each .

5. CONCLUSION

This paper describe a novel semi-systolic array architecture for real time Disrete Wavelet Transform processing of gray level image. The architecture maximizes concurrencies in computing transform coefficients and also maximizes processing elements utilization factor up to 100% ,thus, reduces the dimension of the array implementation. The regularity and modularity of the array and simplicity in control scheme makes it easy to be implemented in today's hardware technologies.

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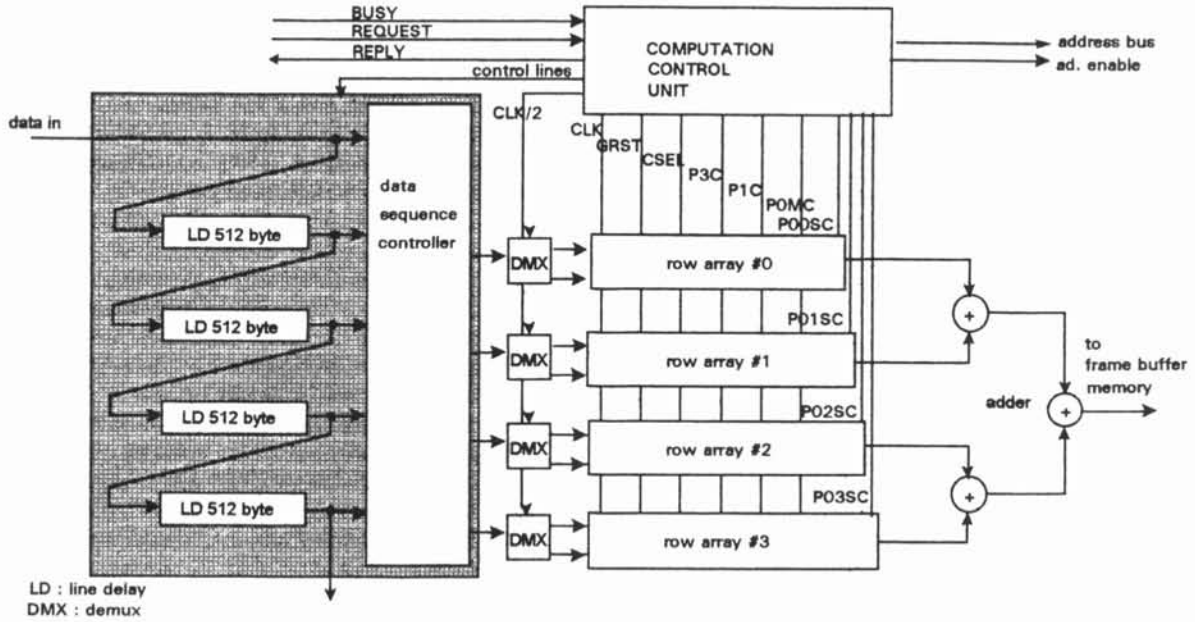

figure 1. discrete wavelet transform processor architecture

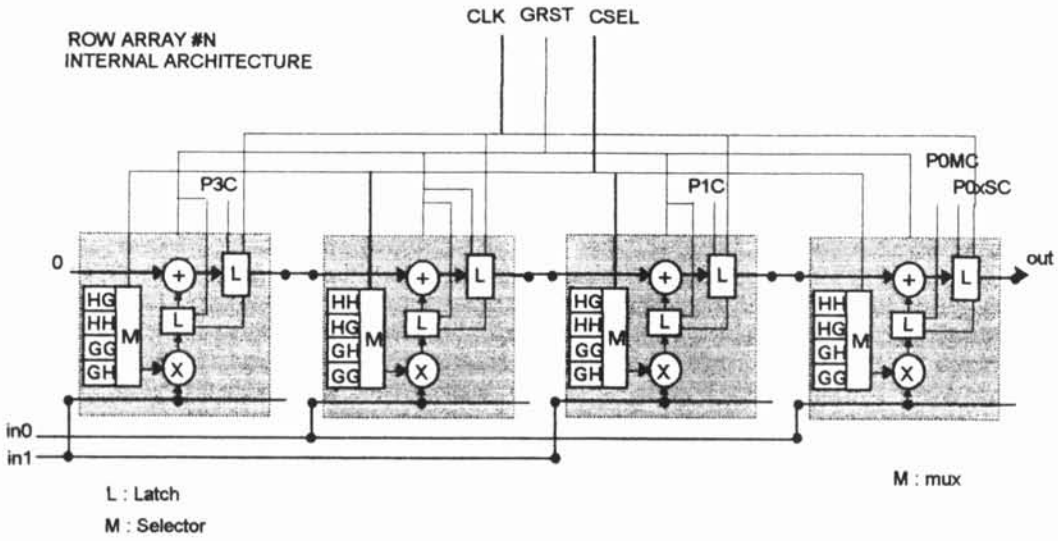

figure 2. row array internal architecture