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Automated Inspection of Printed Circuit Board Patterns Referenced to CAD data

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ABSTRACT

Automated detection of defects in printed circuit board patterns for mainframe computers is accomplished by a system which compares PCB patterns with corresponding CAD data. High speed fluorescence detection is achieved, using highly efficient fiber optic illumination. A simplified reconstruction technique provides precise images. A binarization method that uses maximum and minimum detection along with constant binarization allows detection of narrow cuts and thin shorts. A bit pattern generator produces a bit-mapped design data image from vector format CAD data. A partitioning and dividing technique reduces the design data image to finer bit images to be adapted to those detected by four acquisition systems. To overcome the inevitable distortions in PCBs, stretched or contracted patterns are compensated by dynamically changing pixel size. A proposed defect fatality recognition technique examines not only defect size, but also the relationship with nearby patterns. As a result, only harmful defects are recognized as defects. Fatality is recognized asynchronously in a stand-alone image processor, so it does not waste inspection time. This state-of-the-art automated inspection system can detect short circuits as small as 7μm wide in 4.5 min. on a 600x800mm PCB.

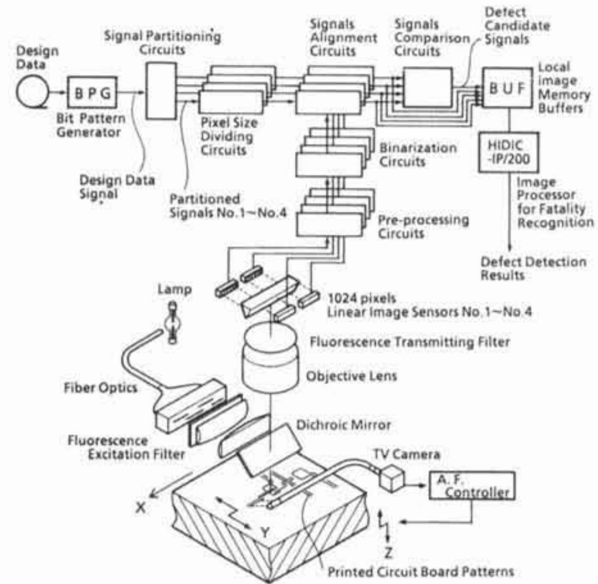


Fig. 1 Configuration of the Inspection System.

1. INTRODUCTION

Printed circuit boards (PCBs) are fundamental components in all electrical equipment and should therefore be free from flaws. Mainframe computers use PCBs which consist of around 50 layers, each of which should be inspected before lamination. A layer has electric circuit patterns formed by chemical deposition of copper on both sides of a substrate. The substrate is made of organic material such as polyimide with glass fiber reinforcement. The typical pattern width is 70μm and the size of a layer is around 600x800mm. Visual inspection of a layer is prone to errors and would take several hours. Therefore, automated inspection of such patterns during manufacture is essential.

Several techniques are used to detect defects in automated inspection systems [1-5]. A typical technique is the design rule method which only detects irregularities in the design rule of PCB patterns. But it can fail to detect defects whose shape is similar to the normal pattern. The comparison method is more reliable, and the most reliable method is to compare the pattern with its CAD data. Since the CAD is used to compose a photomask pattern for each PCB layer, that data should be the best reference pattern for inspection by the comparison method. However, precise alignment, which is often difficult for large PCBs, is required when using comparison method. There is unavoidable stretch or contraction on the order of 100μm in the manufacturing process.

We developed a system that identifies defects by comparing the actual patterns with those electronically generated from the CAD data. In order to ignore above distortions on PCBs, the system uses a new alignment technique that dynamically changes pixel size to align patterns.

Defect fatality recognition is also developed. Previously, detected defects were evaluated by human whether they should be corrected or could be ignored. For example, a defect between lines is a serious problem, but one of the same size in a blank area (no patterns nearby) can be ignored. Our system employs stages of defect detection: defect candidate detection by comparison, and defect fatality recognition by a signal processing unit that analyses the areas near the candidates. Thus, only fatal defects are detected in a practical detection time.

2. PATTERN DETECTION

2.1 IMAGE ACQUISITION

The precise image acquisition required for defect detection is achieved by using the fluorescence detection method. In this method, the fluorescence generated by the PCB substrate when illuminated by violet light is detected. This is suitable for exact pattern acquisition for PCBs because it detects the pattern as a silhouette, and surface conditions do not affect the image [2].

Optical fiber is used to illuminate the PCB with light that is generated by a high pressure mercury lump (Fig. 1). The outlet of the fiber is square in shape so as to illuminate the inspection area effectively. Four linear sensors are used for detection. They are configured to act as a single, four-times-longer sensor with a triangular prism. A high-speed r' 1.6 lens whose field of view is more than 40 mm at magnification one, was developed. A pixel size for inspection is 10μm. Previously, the fluorescence detection method required laser illumination to obtain sufficient light power [6], but the above technique together with a low noise sensing amplifier allows use of ordinary light. The stage that carries the PCB can move in the Y-direction continuously because linear image sensors are used.

2.2 PREPROCESSING

Since four sensors are employed, detected signals are processed in parallel. Two major functions of preprocessing circuits in Fig. 1 are shading compensation and modulation compensation.

(1) SHADING COMPENSATION

The transfer function of the optical system, including the lighting system, and differences in the sensitivity of sensors are compensated. The brightest and darkest images are detected first, and then the head-amplifier gain is determined for each pixel. This shading compensation stabilizes the detection signal over the entire detection area. The system employs four linear sensors to widen the acquisition area, so this compensation helps to guarantee detection sensitivity.

(2) MODULATION COMPENSATION

The substrate material of PCBs is translucent, so the detection signal is determined by not only the illumination power at a certain position but also by the power in nearby areas. Less fluorescence is generated when there is a pattern nearby than when there is not. Thus, patterns that have narrow gaps often result in low modulation and the detected image does not represent the actual shape of the pattern. It should be noted that in comparison referenced to CAD data the reference pattern is so nearly perfect that this kind of small distortion cannot be allowed.

We modeled this phenomena as a transformation F, which is described as fluorescence generation. PCB pattern U is transformed to detected pattern V by transfer function F (Fig. 2). F is a convolution of U and point-spread function D, because fluorescence is generated isotropically from the organic PCB substrate. If the pattern exists, it blocks the illumination and no fluorescence is generated at that point. Instead of applying the deconvolution of V with the inverse function of F, we introduced a function C. Assume V' to be the improved pattern signal,

$$V' = C \times V$$

where,

$$C = \frac{V}{S}, \qquad S = D \otimes V. \tag{1}$$

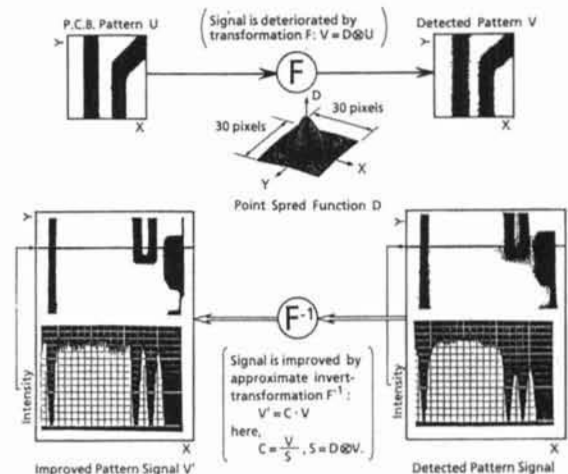


Fig. 2 Improvement of Detected Pattern Signal.

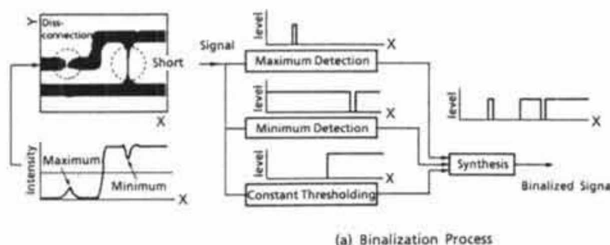
Deconvolution then becomes a simple multiplication of C and V, and we obtained the improved pattern signal V'. In Figure 2, the narrow gap (two bright portions on the right in the waveform) has the same intensity as the substrate with no pattern. Thus, an improved image is obtained in real time using simple hardware comparing with that of a strict deconvolution, which needs an operation in a spatial frequency domain.

2.3 BINARIZATION

Even if modulation compensation is applied as described in the previous section, the signal detected from slight defects is small. As shown in Figure 3, the shape of the detected signal for a disconnection is a small hill, and that for a short is a small valley, so conventional binarization alone cannot detect these small defects. We therefore use convexity and concavity of the detected signal, which represent slight defects, by incorporating an evaluation function F_α, as in equation (2) for the example of x-axis ($\alpha = 0$).

$$F_\alpha(x, y) = P(x, y) - (P(x-\lambda, y) + P(x+\lambda, y)) \tag{2}$$

In Eq. 2, P(x,y) is the intensity of the detected signal at point (x,y), where λ is a constant. In the same manner, F_α is evaluated in four directions (α= 0, 45, 90 and 135 degrees), and if F_α exceeds a certain value, the maximum output (or minimum output) is generated. By synthesizing these maximum and minimum outputs with the result of conventional binarization, slight defects can be detected stably and exactly.



(a) Binalization Process

Fig. 3 Signal Binalization Method.

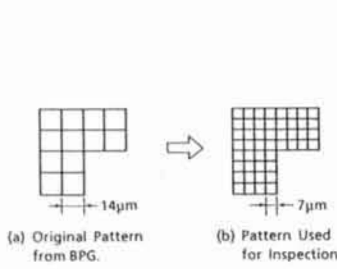


Fig. 4 Division of Pixel Size of Design Data Pattern.

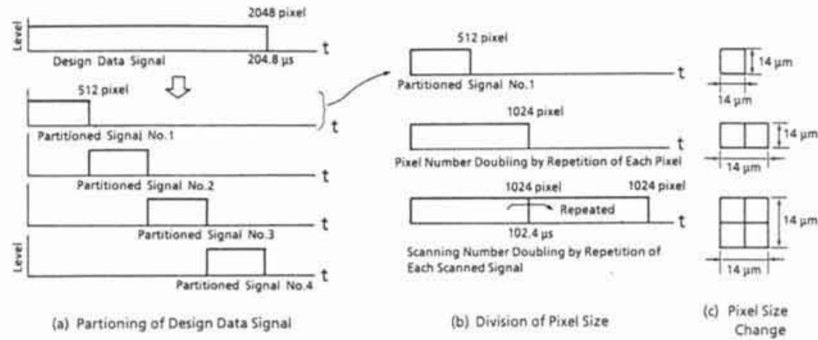


Fig. 5 Processing of Design Data Signal

3. DESIGN DATA PATTERN

Our system identifies defects by comparing the detected PCB patterns with a pattern electrically generated from the CAD data used to manufacture the PCB. The reference pattern, which is a bit-mapped image calculated from the CAD vector data, is generated by a bit pattern generator. The partitioning circuit and dividing circuit reduce the original pattern to finer bit images.

3.1 GENERATION

The detected pattern is compared with design data pattern generated from the CAD data. That data, which is used to make the photomasks for the PCB, is vector data that represents the length and the width of patterns, their position, and so on. For comparison, we need bitwise pixel data (2 dimensional bit image) because the detected pattern is a flow of data corresponding to pixels from the linear image sensors. The BPG (bit pattern generator), which was originally developed for a photomask inspection system[8-9], is used to produce the bit image.

3.2 PARTITIONING and DIVIDING

In order to reduce the processing load on the BPG, partitioning and dividing technique are developed. They make it possible that the CAD data pixels are four times as large as those of the detection pattern, and generation rate of BPG can be 10 MHz for a 40 MHz inspection rate..

The reference pattern from BPG is a time-dependent signal for 2048 pixels. The detection pattern is a set of four signals, each of which is for 1024 7μm pixels. For the reference pattern to match the detection pattern, the original pattern from the BPG is partitioned to four elements (Fig. 4). Figure 5 illustrates this organization of CAD data: (a) shows how a scan of the design data signal matches the four elements of the sensor. Each signal has 512 14μm pixels. In (b), each pixel of the partitioned signal is doubled in time and then repeated in the next scan. (c) shows how the design data signal changes as pixel size changes. These transformations are performed by an electrical circuit in real-time. There is no problem using course pixels, such as 14μm in size, for CAD data because that data does not contain any fine information.

4. ALIGNMENT

(1) Y direction

Since linear sensors are being used for high speed inspection, a PCB is scanned in the Y direction continuously. When design data pattern of length L is compared to the corresponding detected pattern of length L', the number of scans for each pattern must be equal (Fig. 6). This implies that the pixel sizes of design data and detected pattern data should differ according to L and L'. Assume Δ to be the pixel size of the design data and Δ' to be that of the detected pattern. We obtain,

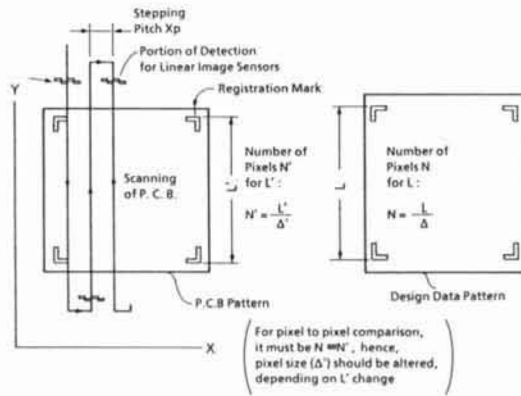


Fig. 6 Scanning Mode of P.C.B., Pixel Size Δ' for P.C.B. and Δ for Design Data.

$$\frac{L}{\Delta} = N, \qquad \frac{L'}{\Delta'} = N. \tag{3}$$

L' differs with the specimen, so we have to measure L' using the alignment marks on the PCB before each inspection. Then Δ' should be modified to satisfy EQ. 3 for each PCB. Here Δ' is determined through measurement by a linear encoder set on a stage. The resolution of Δ' is the same as that of the linear encoder, 1μm in our case. Therefore Δ' is usually 7μm and sometimes 8μm so that the number of pixels in L' equals to N. For example, when L' differs from L by 100μm, Δ' is 8μm per 1000 times. In this method, only the stretched PCB can be aligned, so the pixel size Δ of the design data should be set to make L equal to L' of the smallest PCB.

(2) X direction

The sensors are moved X_p in the X direction after each Y-direction scan. The pitch X_p is changed according to the stretching or contraction of the PCB. The difference from the nominal value is calculated by measuring the position of the alignment mark. Thus, the overlap of each scan differs among the PCBs under inspection.

(3) Alignment with a memory image

Above alignments are coarse ones, so finer alignment is required. The design data pattern and the detected pattern, which are stored in memory within a particular error, are shifted by certain X, Y coordinates. Then the points where the sum of the exclusive OR is minimum defines the aligned position. In signals alignment circuits as shown in Fig. 1, this calculation made in parallel and in real time.

5. DEFECT DETECTION

The aim of the inspection system is to discover defects that may cause an electrical circuit malfunction. However, machines detect errors only according to their criteria, no matter whether the error is fatal or non-fatal. A more intelligent system has been desired. We employed two stages of defect detection and developed a more sophisticated defect detection as a step towards such a more intelligent system.

5.1 DETECTING CANDIDATES

The first-stage result of the algorithms is only a list of defect candidates. Two algorithms are used in this stage.

(1) Algorithm 1: Detecting slight defects.

As shown in Fig. 7 (a), the operator extracts smaller portions than the pattern width from detected pattern and design data pattern, and then these features are compared for the two images. Mismatches are defect candidates. This technique allows detection of defects finer than the pattern width or the alignment error. A normal pattern has the same feature as the design data pattern do, so it will never be taken as a defect.

(2) Algorithm 2: Detecting large defects.

Design data pattern is expanded or contracted (Fig. 7(b)). If the expanded pattern can cover all of the detected pattern, or all of the contracted pattern is in the detected pattern, there are no defects. Otherwise, the portion is a defect candidate.

5.2 DEFECT FATALITY RECOGNITION

The above algorithms may detect a variety of defect candidates. The leftmost columns in Fig. 8 are defects which have the same shape, but different patterns nearby. Defect A is extended to another line, but defect B is not. Concerning harm to electric circuits, defect A may become a short circuit, and is thus fatal. Defect B, however, can be safely ignored. The criteria of defects are shown in Fig. 8. These criteria were used by humans; they were time consuming and required expertise. In order to determine fatal defects, we developed defect fatality recognition.

When a defect candidate is obtained with the above algorithms, partial images (design data pattern, detected pattern, and the defect candidate pattern) are stored in buffer memories. The size of the images is 256x198 pixels. The system has a stand-alone image processor (HIDIC-IP/200). The images are transferred from the buffers to the image processor, and analyzed in detail for defect fatality. When one set of images has been analyzed, the next set is transferred.

Defect fatality is recognized as shown in Fig. 9. Since the criteria differ for a pad and for a pattern, pad areas and line areas are extracted from the design data pattern. After determining the relationship regarding distance between a defect candidate and an extracted pad or line area, the candidate is categorized as a defect on a pad, a defect on a line, or an isolated defect. The criteria are defined in detail for each category, so the area, size, pattern width or gap, or any other suitable characteristic may be measured to determine fatality. The recognition is complicated and requires several tens of program steps, but the image processor runs asynchronously to the main system, and it only analyzes defect candidates in a small image area, so it does not affect inspection time.

6. INSPECTION SYSTEM and SYSTEM PERFORMANCE

We used the above techniques to develop the automated inspection system shown in Fig. 10. Leftmost cabinet is a BPG. A magnetic tape is used to transfer CAD data to the BPG. A cabinet next to BPG is a control unit that has a monitor to display inspection result. A PCB under inspection is placed on a X-Y table of the right unit. The inspection time is 4.5min. for a 600x800 mm PCB.

(a) Algorithm 1 : Extraction of Small Portion and Comparison.

(b) Algorithm 2 : Matching of Detected Pattern with Swelled / Shrinked Design Data Pattern

Fig. 7 Algorithm for Defect Candidate Detection.

Fig. 8 Criteria for Fatal Defect Judgment.

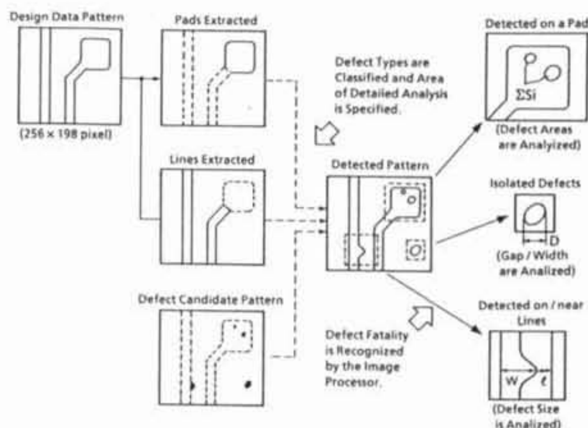


Fig. 9 Process of Defect Fatality Recognition.

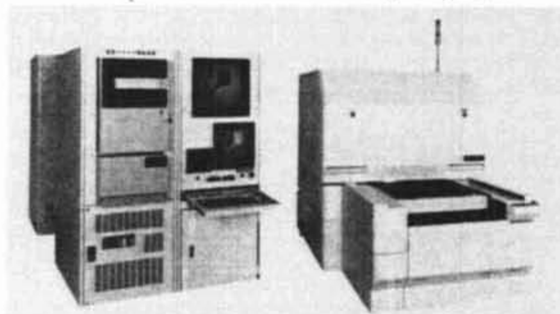


Fig. 10 Developed Inspection System.

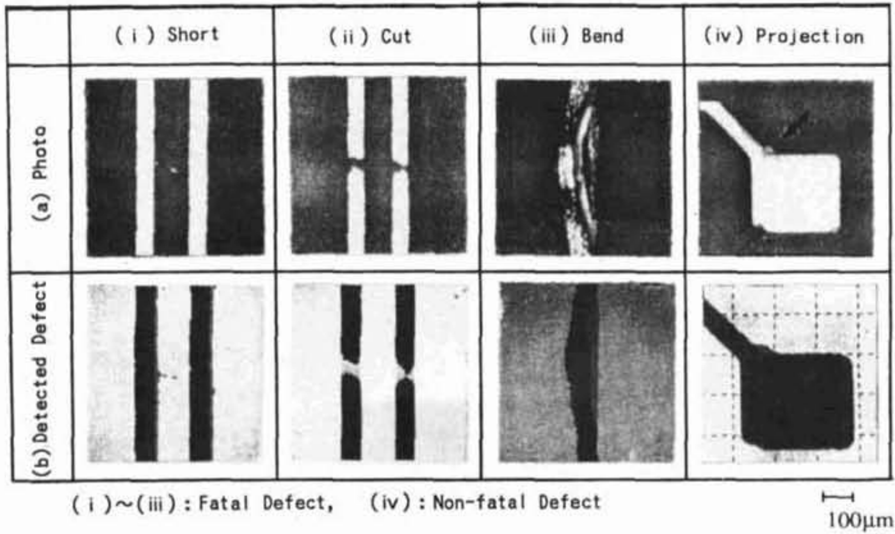


Fig. 11 Examples of Detected Defects.

The system can detect harmful defects even if their shape resembles normal patterns. Examples of defects detected by the system are shown in Fig. 11. Photographic pictures of defects are shown in (a). Binarized images of (a), which are obtained with the system, are superimposed on corresponding design data image, and they are shown in (b). Overlapped portion is dark. The system detects 7µm hairline short, cut, abnormal line, pattern variations, and other such defects accurately. Notice that a bent pattern is a fatal defect, because the defect means that a copper pattern comes off a substrate and it may cause a serious problem. It is also noted that the defect shown in Fig. 11 (iv) was detected by comparison, but it was eliminated by defect fatality recognition: as small defect as that shown in Fig. 11 (iv) should be detected, however, criteria for fatal defect judgment allows that size of deformation on pads.

7. CONCLUSION

A state-of-the-art system for automated detection of defects in printed circuit board patterns for mainframe computers is described. This system compares detected patterns with corresponding patterns, which are electrically generated from the CAD data. Several techniques are developed: modulation compensation, binarization that focuses on detecting narrow gaps and thin shorts, alignment technique that allow inevitable distortions in a PCB, defect fatality recognition, and so on. As a result, highly reliable inspection system, which can detect short circuits as small as 7µm wide within 4.5 min. in a 600x800mm printed circuit board, is accomplished.

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REFERENCES

[1] Y. Hara, N.Akiyama, K.Karasaki, "Automatic Inspection System for Printed circuit Board," *IEEE Trans. Pattern Anal. Mach. Intell.*, vol. PAMI-5, no.6, pp.623-630, Nov. 1983.
[2] Y. Hara, H.Doi, K.Karasaki, T.Iida, "A System for PCB Automated Inspection Using Fluorescent Light," *ibid.* vol. PAMI-10, No.1, pp.69-78, Jan. 1988.
[3] K.Landman, "Overview of AOI Systems," *PC FAB.*, pp.17-34, Nov. 1988.
[4] J.L.C.Sanz, A.K.Jain, "Machine-vision techniques for inspection of printed wiring boards and thick-film circuits, " *J. Opt. Soc. Am.*, vol.3, No.9, pp.1465-1482, Sep. 1986.
[5] G.A.W.West, "A System for the Automatic Visual Inspection of Bare-Printed Circuit Boards," *IEEE Trans. Syst., Man Cybern.*, vol.SMC-14, No.5, pp.767-773, Sep./Oct. 1984.
[6] Y.Hara, K.Karasaki, M.Wada, S.Shinada, T.Furutani, N.Minatani, S.Kitamura, "High Speed P.C.B. Inspection System utilized Ar Laser Illumination and Fluorescence Detection (1)," *Proc. 70th National Convention Record, Institute of Electronics, Information and Communication Engineers, Japan*, No.2533, vol.7 p.133, Apr. 1987 (in Japanese).
[7] H.Doi, A.Sase, M.Fukunaga, T.Nagata, Y.Sakurai, M.Suzuki, M.Kogure, "High Speed P.C.B. Inspection System utilized Ar Laser Illumination and Fluorescence Detection (2)," *ibid*, No.2534, vol.7 p.134, Apr. 1987 (in Japanese).
[8] K.Nakahata, T.Hamada, Y.Nakagawa, M.Nomoto, Y.Hashimoto, K.Karasaki, "High-speed Two-dimensional Pattern Generator using Multi-DSPs' Parallel Processing for Pattern Inspection of PCB Photomasks," *Trans. Inst. Electrical Engineers of Japan*, Vol.110-D, No.7, pp.781-790, 1990 (in Japanese).
[9] T.Hamada, K.Nakahata, M.Nomoto, Y.Nakagawa, "Automated Pattern Inspection System for PCB Photomasks Using Design Pattern Comparison Method," *IECON '90*, vol.1, pp.780-785 (1990).