SATELLITE IMAGE PROCESSING USING CELLULAR ARRAY PROCESSOR(CAP)

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ABSTRACT

Since the successful launch of the Japan Earth Resources Satellite-1 (JERS-1) in February of 1992, it has been sending back images of the earth for various studies, including the investigation of earth resources, the preservation of environments, and the observation of coastal lines.

Because images sent from the JERS-1 have very high resolution, their analyses require the power of a high-speed image processor. For this purpose, the ERSDIS, a cellular array processor based system, has been adopted. The cellular array processor consists of 4096 processing elements in a two-dimensional array and it's suitable to process large-scale image data at a high-speed.

This paper describes the structure of the ERSDIS, and also the details of the cellular array processor unit used.

INTRODUCTION

JERS-1, a product of a joint project by the Ministry of International Trade and Industry (MITI) and the National Space Development Agency of Japan (NASDA), has been successfully launched in February of 1992.

Two kinds of sensors are employed in the JERS-1, a conventional optical sensor, the OPS, and a microwave sensor, the SAR. The SAR is capable of detecting forests, deserts and seas at a spatial resolution of 18m, while the observation width can be extended up to 75km.

Images produced by both the OPS and the SAR are processed at the Earth Resources Satellite Data Analysis Center (ERSDAC). The processing system used is called the Earth Resources Satellite Data Information System (ERSDIS). CAP, a cellular array processor serves as the main processor unit for high-speed image processing in the ERSDIS.

This paper describes the ERSDIS's system configuration, the CAP's features and the SAR's image.

ERSDIS SYSTEM

The ERSDIS was developed to provide a JERS-1 data utilization system for effective applications dedicated to resources user. Figure 1 shows the system's structure, which consists of three subsystems.

1. Data Retrieval & Distributed Subsystem(ERS-DRS)
2. Data Processing & Archiving Subsystem(ERS-PRS)
3. Data Analysis Subsystem(ERS-ALS)

The subsystems are linked by a high-speed LAN. The functions of the ERS-DRS and the ERS-ALS are also described in Figure 1.

To obtain information relating a satellite image, a user first accesses the ERS-DRS to place his order. While the processing and outputting of images are executed by the ERS-PRS, their analyses are carried out by the ERS-ALS.

The main features of the ERSDIS are as follows.

1. High-speed image processing
   A cellular array processor (CAP), which consists of 4096 processing elements, can process large satellite image at a high-speed. Details of the CAP's architecture are described later.
2. Wide variety of user interface
   A user can access the ERSDIS using remote terminal via telephone line. In addition, many medium including MT, cassette MT, floppy and paper are prepared for output of image.
3. Operator Saving
   Two automatic storage systems are adopted to save operating overheads.

The next section describes the ERS-PRS.

ERS-PRS SUBSYSTEM

The ERS-PRS mainly consists of the following five devices.

1. Automatic storage: A tape which includes raw data is selected, and the raw data is read from the tape

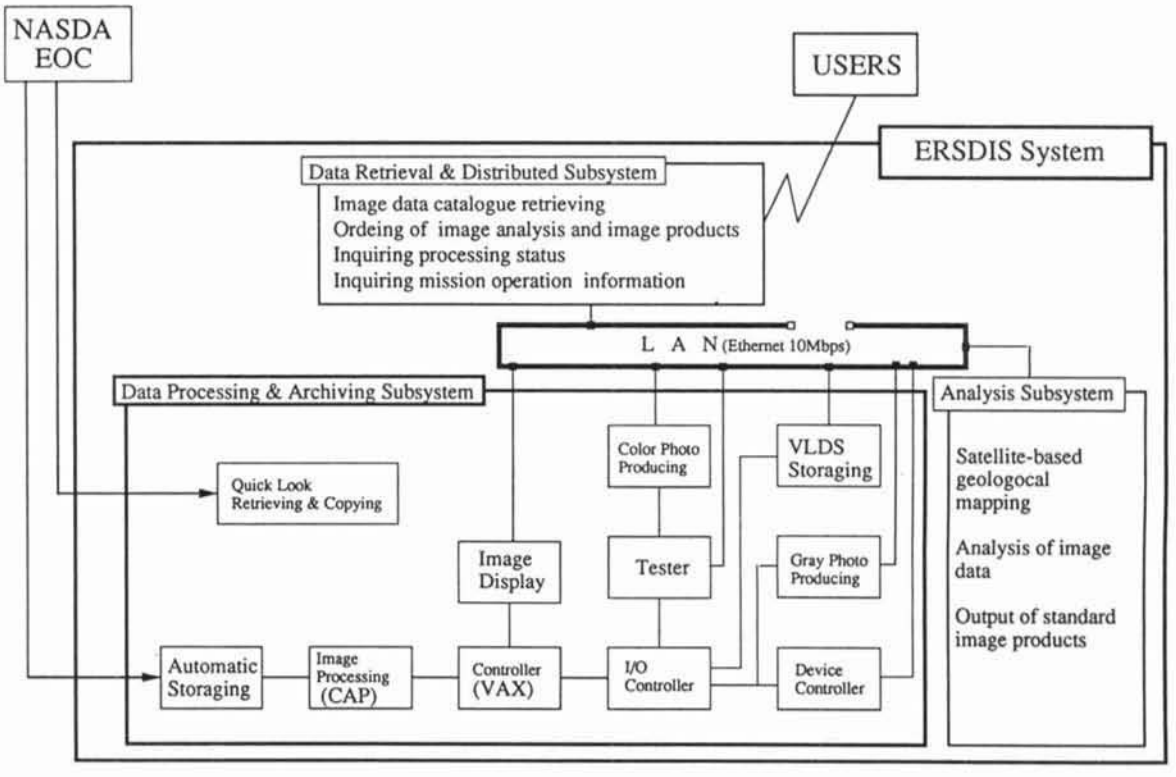

Figure 1: Structure of ERSDIS system

and sent to the image processor CAP. The processed data is similarly treated in the VLDS Storage. No operator is needed to support this.

2. CAP: CAP processes image data at a high-speed.

3. Controller(VAX): The VAX is a main controller in the ERS-PRS subsystem.

4. Color or Gray Photo Producing: The processed image data is produced by these photo producing. Both color and gray photos are supported.

5. Quick Look Retrieving & Copying: A quick look data is retrieved and copied in this device.

CAP SYSTEM

Cellular Array Processor: In general, cellular array processor consists of thousands of simple processing elements(PE) in a two-dimensional array and it is suitable to process large-scale image data at a high-speed. It has the following features:

1. Image data is processed easily in parallel because the PEs are located in a two-dimensional array.

2. Short-length data of image is efficiently processed in each PE because the PE is simply constructed.

3. It is easy to enhance the system because the PEs are located in a two-dimensional array.

As there are merits in cellular array processor described above, some research have been done [1][2].

On the contrary, however, there are also some demerits in the design:

1. Though the processing speed is fast, data transfer between the PEs and main memory have high overhead.

2. As in other SIMD architectures, it lacks flexibility.

3. Data transfer between distant PEs also exerts high overhead.

CAP resolved these problems [3][4], so it is called an extended cellular array processor.

System Configuration: Figure 2 illustrates the block diagram of the CAP system, which consists of the CAP, SM and CTLP.

The CAP consists of a cellular array unit to perform parallel processing, the PEs controller (PEs Cont.) and the I/O controller (I/O Cont.). The CAP controller (CAP Cont.) controls the whole components of the CAP.

The cellular array unit consists of 4096 processing elements configured into a two-dimensional array. Each PE has an 8 bit ALU, a register file, local memory, two modifiers and control registers.

A program of the CAP is stored in CAP Cont. Scalar operations and program sequence controls are processed in CAP Cont. Array operations are sent to PEs Cont.

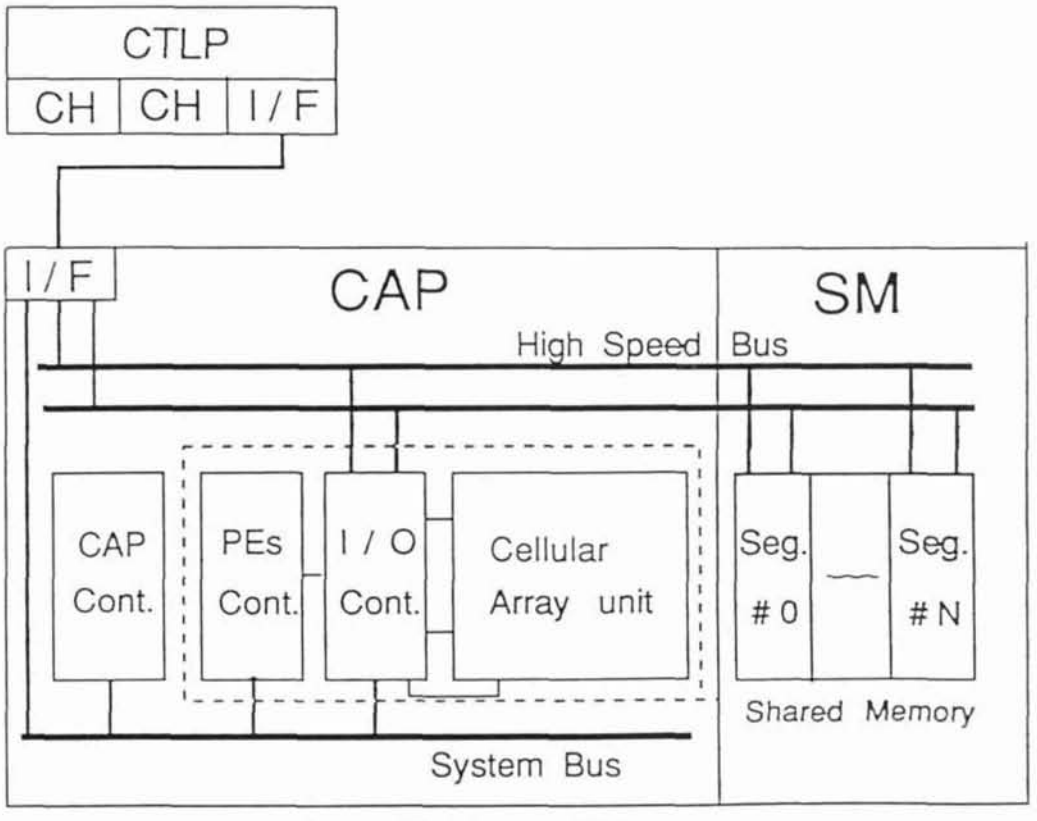

Figure 2: Block Diagram of CAP system

and processed in it. I/O operations are decoded in CAP Cont. and I/O commands are sent to I/O Cont. I/O Cont. controls high speed data transfer between cellular array unit and SM through high speed bus.

Features: The CAP unit has the following features:

- Block pipeline
  Three controllers in the CAP unit, the CAP Cont., the PEs Cont. and the I/O Cont., process each operation independently. Therefore the operations in each processor, the scalar operation in CAP Cont., the array operation in PEs Cont. and the input/output operation in I/O Cont., are processed simultaneously. Using this method, we realize high speed processing. Namely, after dividing the image in SM into the blocks which have the same number of pixels as the PE's, the following process will be executed in parallel.

  1. transferring one block from the cellular array unit to SM,
  2. process next block in the cellular array unit,
  3. transferring the next block from SM to the cellular array unit.

  As the image data are divided into blocks which are processed in pipeline style, we call this method "Block Pipeline".

- Operation Modifier
  All PEs receive identical operations from the PEs Cont. Each PE, however, can modify the operations using its own control register and performs different operation respectively. For example,

  1. operation or no-operation,
  2. addition, subtraction or transfer etc.

- Address Modifier
  All PEs receive the same addresses of their register files as well as the operations. Each PE has an address modifier and the address of the register file is modified whenever necessary, such as the normalization in floating-point operation. As a result, the CAP executes floating-point operations of high performance as well as fixed-point operations.

- Broadcast from PE to PE
  Each PE is connected with two to four neighbor PEs. Usually data transfer between PEs is done through neighbor PEs. In addition, CAP has a broadcast function between PEs and it can enable PEs to transfer data by skipping neighbor PEs.

- Two-dimensionally accessible memory (SM)
  SM is a two-dimensionally accessible memory. When we access one rectangle data in SM, we only give the SM three parameters: the location address, the row length and the column length of the rectangle data. After that, high speed data transfer of the rectangle data is done. CAP processes high speed image processing using these features.

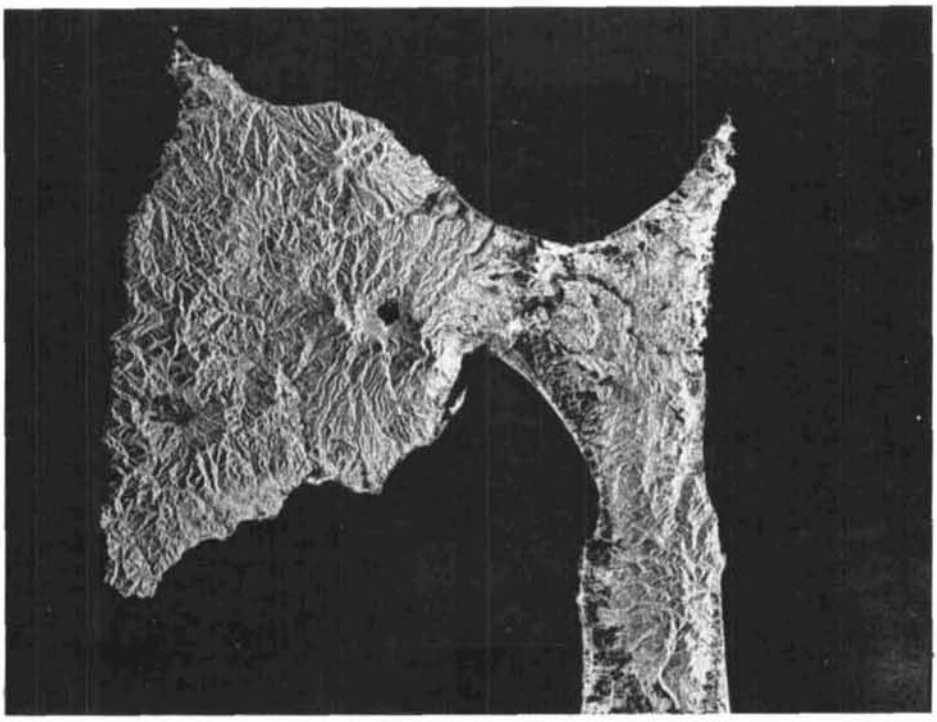

Figure 3: SAR Reproduced Image

courtesy of MITI/NASDA

SAR Reproduce Processing

We reproduced SAR(Synthetic Aperture Radar) image. Figure 3 illustrates the reproduction image from the hologram processed by CAP. It is an area of Shimokita Peninsula in Japan.

Conclusion

In this paper, we described the ERSDIS's system configuration, the ERS-PRS unit and the CAP unit. CAP is an extended cellular array processor and it's used for high-speed image processing.

This architecture realizes several types of parallel processing such as block pipeline, operation modifier, address modifier, broadcast from PE to PE and two-dimensionally accessible memory.

Owing to these features, images sent from the JERS-1 can be processed at a high-speed.

A product distribution will be started in autumn of 1992 at the ERSDAC's Data Center, Japan.

References

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